# SHARING

## SELF-ORGANIZED HETEROGENEOUS ADVANCED RADIO NETWORKS GENERATION

D7.2

Selection of key algorithms and technologies with Integration into platforms

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**Abstract:**

SHARING project develops a number of algorithms and technologies in WPs 3 to 5. Specific scenarios derived from these studies have been selected in deliverable D7.1 as candidates for implementation in Proof of Concept (PoC) test-beds. In this deliverable, the key algorithms and technologies that will be integrated in the various demonstrators are described in detail, as well as the building blocks of the corresponding PoCs.

Five use cases are under implementation, on the following topics:

- eMBMS and D2D relaying :
  - eMBMS relaying for coverage extension of eMBMS multicast-broadcast services,
  - Device-to-device (D2D) communications for content delivery reusing uplink resources
- Cooperative Multipoint (CoMP) transmission and Multiuser-MIMO (MU-MIMO) coupled with interference rejection in User Equipment (UE),
- Advanced RF architectures and antennas in support of Carrier Aggregation (CA),
- WIFI Offloading,
- FPGA reconfigurability for low-power filter banks implementation.

**Keywords:** Experimental Validation, Platform Building Blocks, eMBMS multicast-broadcast services, D2D, Cooperative Multipoint (CoMP), Carrier Aggregation (CA), WIFI Offloading, FPGA reconfigurability, Filter banks implementation.

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# TABLE OF CONTENTS

# LIST OF FIGURES

**AUCUNE ENTREE DE TABLE DES MATIERES N'A ETE TROUVEE.**

# LIST OF TABLES

# EXECUTIVE SUMMARY

In SHARING deliverable D7.1 "Selection of scenarios for proof of concept (PoC) testbeds and recommendations on key building blocks for implementation", the use cases to be considered for experimental validation were described. These scenarios that correspond to algorithmic/technology studies carried out in other WPs are the following:

- Relaying in two different contexts: eMBMS relays for coverage extension of eMBMS multicast-broadcast services and Device-to-device (D2D) communications for content delivery reusing uplink resources (WP5)
- Cooperative Multipoint (CoMP) transmission coupled with interference rejection in User Equipment (UE) and Multiuser-MIMO (MU-MIMO) (WP3)
- Advanced RF architectures in support of Carrier Aggregation (CA) (WP3)
- WIFI Offloading (WP4)
- FPGA reconfigurability for low-power filter banks implementation.(new work that was not included in D7.1)

D7.1 also gave preliminary descriptions of the technologies used to build the PoC demonstrators, specifying whenever relevant the required modifications to existing hardware and software, as well as an insight on the integration methodology.

In the present deliverable, the key algorithms and technologies that will be integrated in the various demonstrators are described in detail, as well as the building blocks of the corresponding PoCs.

The considered use cases are as follows:

**eMBMS relaying and D2D transmission**
Two demonstration scenarios covering eMBMS relaying and D2D transmission are proposed. The first and highest-priority scenario corresponds to the case of a macro-cell eMBMS transmission with a multi-relay network to extend coverage to dark zones. The relays operate either on a secondary component carrier or on an orthogonal MBSFN-area in a region around the relays. It will consist of specially made relay-nodes comprising conventional eMBMS UE receivers and eMBMS eNB transmit functions. If available, a commercial eNB and commercial end-user UEs will be used at the extremities of the demonstrator. The second scenario consists of specially-made D2D transmission for intra-cell D2D transmissions reusing the uplink carrier frequency. It will employ TDD framing. Both broadcast and scheduled D2D transmission are considered and the latter focuses on application scenarios for relaying of cached content to nearby terminals.

**CoMP (Cooperative Multi-Point), and MU-MIMO (Multi-User MIMO) with interference rejection capability at the receiver**.

Different algorithms for interference mitigation have been considered and evaluated in [19]. A real-time hardware in the loop demonstrator was presented to further validate this concept [1]. SL-MMSE and IA-ML have been selected for implementation for their respective properties of low complexity and best performance. A preliminary complexity evaluation is first performed, and concludes that IA-ML is significantly more complex than SL-MMSE. Both algorithms are then evaluated for implementation on a Xilinx Kintex-7 FPGA platform to refine these preliminary complexity estimates. Finite precision register specifications have been derived by simulation for both algorithms and an implementation of the algorithms on 12-bit input/output registers has eventually been performed. The proposed implementation meets the constraints of the chosen Xilinx Kintex-7 platform and its implementation complexity is compared to a standard LTE design block: the 1024-point FFT used in the 10MHz Mode. The result shows that apart from the FPGA DSP resources, the algorithm maps very well into the platform. This suggests that DSP resource sharing should be further investigated to reduce the amount of necessary DSP resources and therefore the cost of implementation of the CoMP algorithms.

**Carrier Aggregation (RF and Antenna)**

A reconfigurable and flexible bandwidth RF front-end to support intra-band and inter-band CA was designed and the building blocks of the corresponding PoC are presented. The main goal of this PoC is to provide energy savings adjusting the RF output power level according to the number of component carriers (CCs). This hardware prototype enables the combination of up to 3 CCs which will be enough to evaluate its performance studied previously in WP3. LTE band 7 was selected to perform intra-band CA and LTE band 20 and LTE band 7 to implement inter-band CA. Details about some evaluation boards of

the building blocks are described presenting preliminary results of the quadrature modulators, the reconfigurable oscillators and the reconfigurable power amplifier at band 7 tested at different operating points.

To support Carrier Aggregation, a dual band operation frequency agile small cell antenna has been designed. This antenna, being capable of adapting its bandwidth to the active channel configuration, has its instantaneous bandwidth reduced compared to a regular base station. This bandwidth reduction has allowed the miniaturization of the antenna system. A detailed description of the technology used for the prototype currently being built is available in this document. Also, the antenna system being relative small, antenna measurements must be carried out with precaution. Some studies dealing with the cable impact during the measurement are presented in this document.

**Wi-Fi offloading**
Operators are looking for cost-effective solutions to overcome the capacity bottlenecks likely to emerge in high contention traffic scenarios due to the substantial increase in the mobile data traffic volume. Wi-Fi Offloading method aims to propose a long-term solution for the inevitable capacity bottleneck. Accordingly, operators are already expanding their networks to take advantage of Wi-Fi offloading and free-band communications. One of the open research issues regarding Wi-Fi offloading is the optimal selection of the potential wireless networks to connect in heterogeneous networks. To this extent, a new centralized Wi-Fi offloading platform is designed and implemented using a multiple attribute decision making algorithm. The utilized algorithm within the platform is shown to enhance system wide channel utilization of heterogeneous networks, thereby increasing end-users' quality of service and experience

**FPGA Dynamic Partial Reconfiguration for reconfigurable and Low Power Filter Bank Implementation**

A reconfigurable linear-phase, low-complexity digital filter bank based on modified coefficient decimation method and spectral parameter approximation was proposed for spectrum sensing in the CR-LTE system. The main objective is to implement this filter using FPGA dynamic partial reconfiguration technique which allows very low power consumption and a reduced reconfiguration time. The implemented filter is capable of extracting channels of uniform and non-uniform bandwidths corresponding to multiple wireless communication standards from the digitized wideband received signal.

In conclusion, this deliverable paves the way towards the next steps which are the integration of these building blocks and the final Proof of Concept validation.

# 1 Introduction

### Objective and structure of the document

In SHARING Deliverable D7.1 "Selection of scenarios for proof of concept (PoC) testbeds and recommendations on key building blocks for implementation", the use cases to be considered for experimental validation were described. These scenarios and the corresponding WPs are as follows

- Relaying in two different contexts: eMBMS relays for coverage extension of eMBMS multicast-broadcast services and Device-to-device (D2D) communications for content delivery reusing uplink resources (WP5)
- Cooperative Multipoint (CoMP) transmission coupled with interference rejection in User Equipment (UE) and Multiuser-MIMO (MU-MIMO) (WP3)
- Advanced RF architectures in support of Carrier Aggregation (CA) (WP3)
- WIFI Offloading (WP4)

In addition, a platform that was not described in D7.1was included here: FPGA reconfigurability for low-power filter banks implementation.

D7.1 gave preliminary descriptions of the technologies used to build the PoC demonstrators, specifying the required modifications to existing hardware and software along with addressing the integration methodology.

In this deliverable, the key algorithms and technologies that will be integrated in the various demonstrators are described, as well as the building blocks of the corresponding PoCs.

# 2 Selection of key algorithms and technologies with integration into platforms

Here we recall briefly the algorithms or technologies that are going to be implemented. Details are referred to D3.x. If D3.x proposed different solutions and only some of them finally implemented, this is the place to explain why.

Then, we describe what is, or what will be the implementation of these algorithms/technologies in HW.

Algorithms/technologies are grouped along the scenarios of D7.1.

## 2.1 Use-case 1: Relaying and D2D

We will consider two demonstration scenarios as described in Figure 1 and Figure 2, with priority given to the eMBMS relay. These scenarios are described in more detail in [1]. The first one corresponds to the case of a macro-cell eMBMS transmission which is relayed on a secondary component carrier to the region around the relay. The relays derive time and frequency synchronization from the macro-cell eNBs and have transmit-only functionality. These ensure coverage of the primary eMBMS carrier in difficulty to reach areas such as large underground zones or heavily shadowed zones, which would limit the global eMBMS throughput if covered by the macro-cell eNB only. The primary target is to serve the MBSFN-area with a very high-spectral efficiency from the macro-cell eNBs which are received by the great majority of locations and add the TX-only relay to cover the difficult-to-reach zones. The relay is a decode-and-forward relay made up of a standard eMBMS-aware UE and the MBMS TX-path of an eNB.

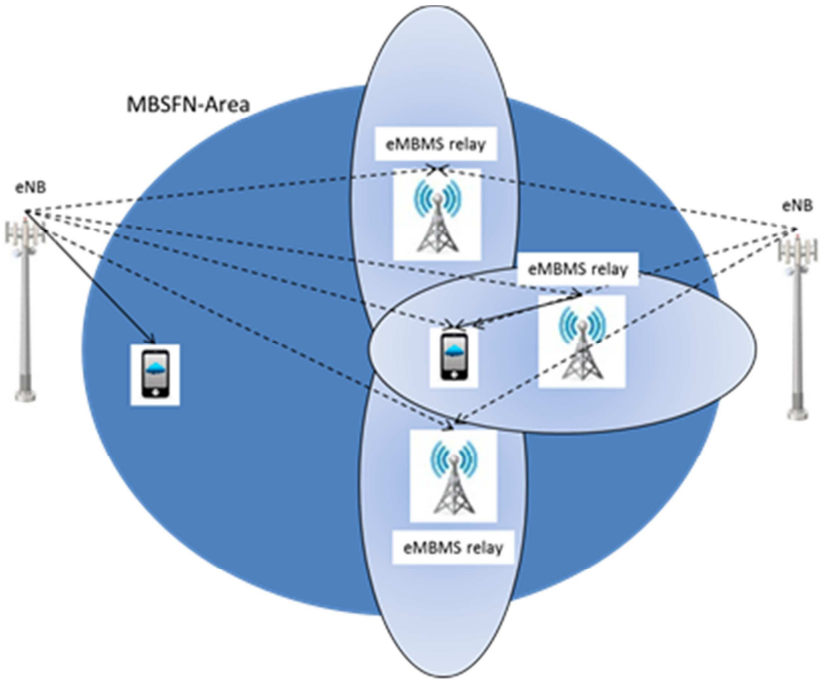


**Figure 1: eMBMS Relay (dual-carrier)**

The second use-case in Figure 2 is more representative of a D2D scenario but can be demonstrated on a similar platform to the first use-case. Here we assume UEs with storage which can be used to offload their content to their local vicinity under the command of the eNodeB which represents at least one Public Land Mobile Network (PLMN) which is aware of the content in the UE relay. The key innovation here is to exploit the uplink carrier for D2D content offload without significantly disturbing the eNodeB's receiver link budget. All UEs must be able to listen to both the downlink and uplink carrier simultaneously.

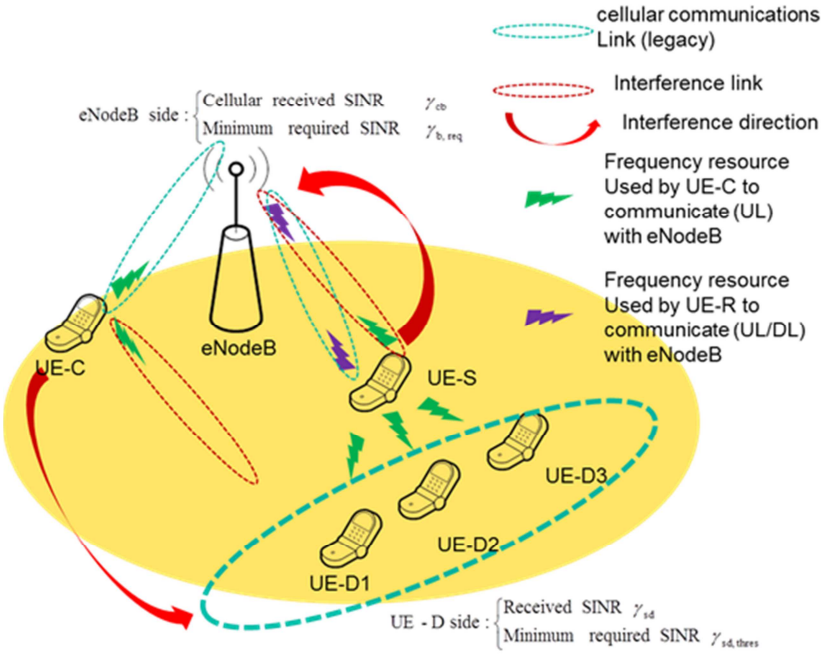


**Figure 2: Use-case 2: Content Delivery (via proximity-based D2D Broadcast)**

### 2.1.1 Selection of algorithm

In both cases we will consider Decode-and-forward relaying where the relaying nodes receive information from the Donor-eNB by the traditional downlink resources and proceed to fully decode the information.

#### *2.1.1.1 eMBMS Relaying*

An *N*-relay case is shown in Figure 3, where *N* will be limited to 2 for demonstration purposes. The MBSFN TX refers to the collection of eNodeBs that are jointly transmitting in a particular MBSFN-area. The relays are assumed to have an aggregate channel supporting as high an MCS as possible. Each relay decodes the downlink eMBMS traffic as a UE and re-encodes on a separate carrier as an eNodeB. In the event that decoding of the downlink signal at the relay is unsuccessful, the corresponding relay will remain silent during that subframe. Synchronization is achieved via the downlink signal of the MBSFN TX which is recovered similarly by all relays. The UE is assumed to be able to switch between the original eMBMS signal and the signal from the distributed set of relays.

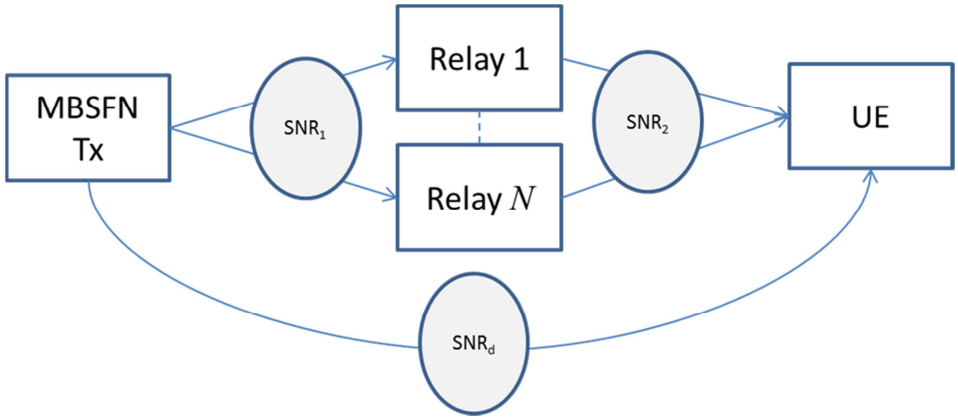


**Figure 3: *N*-relay scenario**

#### *2.1.1.2 D2D for content delivery (broadcast)*

In the broadcast case corresponding to Figure 2, a group of UEs are assumed to act autonomously with respect to the eNodeB in the sense that they use random-access opportunities to transmit in uplink subframes using PUSCH resources. Moreover, they are assumed to exchange sporadic amounts of low-rate information within their group at low-power. These resources are allocated semi-statically by the eNodeB and occupy valid uplink subframes assuming TDD operation in the eNodeB's cell. The transmission strategy will make use of the contention-based access method described in [25]. This method assigns a random-access radio-network temporary identifier (RA-RNTI) to a group of UEs that can communicate via D2D resources. These UEs contend on the resource using only a small number of randomized contiguous PRBs. Randomization in frequency minimizes the impact on the eNodeB and allows reduced contention among the group of UEs. The set of PUSCH resources are dimensioned by the eNodeB (including MCS and number of PRBs). No control information is relayed by layer 2 services (i.e. MAC control elements) in this transmission mode. **Table 1** summarizes the key transmission parameters for contention-based D2D transmission:

**Table 1: Transmission Parameters for Broadcast D2D Transmission**

| **Transmission Property** | **Comments** |
|---|---|
| Scheduling | Each contention-based access (CBA) is semi-statically allocated by RRC configuration. A CBA resource is a pair of physical resource blocks with a given MCS and transmit power. Each UE in the CBA group has a unique cyclic-shift for transmission of the reference signals. |
| Duplexing | TDD |
| Physical Channel | PUSCH |
| Reference Signals | Demodulation Reference Signals (DMRS) with a UE-specific cyclic-shift derived from RRC signaling. |
| Timing advance | None. All UEs using this resource are assumed to transmit their PUSCH signals relatively to their synchronization time determined from the DL eNodeB transmission. All time differences due to propagation delay are assumed to be absorbed by the cyclic prefix or resolved by the receiver of the UEs that are listening. |
| Contention resolution | Contention resolution is reduced by randomized CBA selection and interference mitigation in the receiver using multiple-antennas and or SIC. |

#### *2.1.1.3 Scheduled D2D transmission*

Scheduled D2D transmission can be seen as a form of PUSCH scheduling. UE's are identified by the EPC as relays for content and their local cache is setup and managed by the EPC using a specified method (which for the moment is left FFS). Signaling between EPC and NAS (also FFS) is used to trigger transfer of information to the vicinity of the relaying UE. A total transfer size is negotiated between the EPC and the relaying UE and it is segmented by lower layers (RLC and PHY) as in conventional UE→eNodeB transmissions.

**Table 2: Transmission Parameters for Scheduled D2D Transmissions**

| **Transmission Property** | **Comments** |
|---|---|
| Scheduling | Each scheduled D2D transmission is performed using a special DCI format which comprises the standard PUSCH scheduling information (MCS, PRB allocation, redundancy version index (rvidx)). DCI CRC is scrambled by a UE-specific RNTI corresponding to relay operation, known by both the sending UE and receiving UEs in its vicinity. The resource should be seen as a locally scheduled multicast. |
| Physical Channel | PUSCH |
| Duplexing | TDD |
| Reference Signals | DMRS with a UE-specific cyclic-shift dependent on component signaled in DCI. |
| Timing advance | None. The UE using this resource is assumed to transmit their PUSCH signals relatively to their synchronization time determined from the DL eNodeB transmission. All time differences due to propagation delay are assumed to be absorbed by the cyclic prefix or resolved by the receiver of the UEs that are listening. |
| Power Control | MCS dependent, per PRB base level based on RRC configuration. |
| Feedback indication | ACK/NAK only via PUCCH to eNodeB. ACK/NAK is transmitted using on-off keying (using PUCCH format 1). An ACK from a particular receiving D2D UE is indicated by absence of signal (i.e. binary 0) and NACK by transmission of PUCCH format 1 (binary 1). The rationale is that multiple receiving UEs can transmit simultaneous NACKs which are not disturbed by ACK (i.e. they are orthogonal). This is a common ACK/NAK mechanism to allow multicasting with HARQ. A NAK from at least one UE causes a retransmission. |

### 2.1.2 Platform implementation

The following equipment will be used for demonstration

- An OpenAirInterface (OAI) eNodeB comprising a standard x86 PC, ExpressMIMO2 RF front-end and a high-power amplifier (852 MHz TDD or 2.6 GHz Band38 TDD, 5-10 MHz) for all demonstration scenarios
- 2 OAI-based relay nodes comprising a standard x86 PC and one ExpressMIMO2 (up to 2 ports for UE part and 2 ports for eNB part)
- 1 COTS (Commercial Off-The-Shelf) Rel-10 UE (with eMBMS functionality) for eMBMS-relay scenario
- 2 OAI UEs enhanced for D2D

#### *2.1.2.1 Relay Node Architecture*

The relay node architecture for eMBMS relaying is shown in Figure 4. The UE component of the relay extracts eMBMS information from the DL transmission from the main eNodeB. It regenerates the DL-only necessary control information (PSS,SSS,PDCCH,PCFICH,PBCH,SIB1,SIB2,SIB3,SIB13,MCCH) and

the user-plane (MCH). The other function is to synchronize to the DL transmission in time and frequency in order for multiple relays to collaborate optimally within the MBSFN-area.

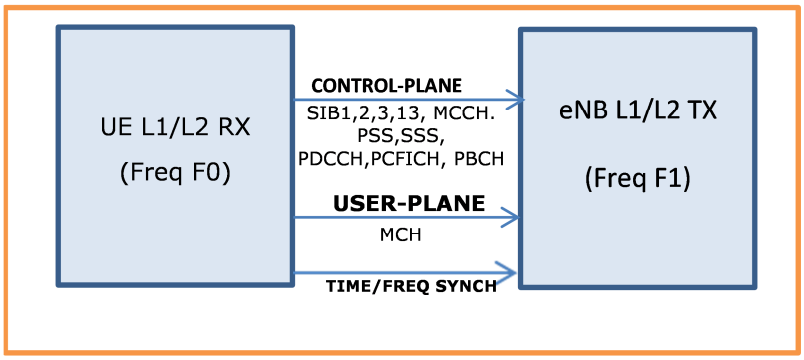


**Figure 4: eMBMS Relay Architecture**

The D2D UE architecture is shown in Figure 5. It comprises a standard Rel-10 UE configured in TDD mode. The DL signaling is augmented by a specific D2D DCI which carries the scheduling grant for a particular D2D UE (Section 2.1.1.3) or a random-access D2D transmission (Section 2.1.1.2) which is used to schedule D2D transmission or reception on the scheduled resources. The procedures related to scheduling, transmission and PUCCH feedback will follow the identical timing to PUSCH scheduling for TDD. PUCCH feedback will make use of a modified physical channel using PUCCH format 1 (on-off keying) to allow for feedback from multiple destinations. The D2D MAC will be transparent (i.e. it will not add control elements) and will make use of unacknowledged RLC (RLC-UM) only. The PDCP entity will be linked to a local cache for D2D information to be relayed.

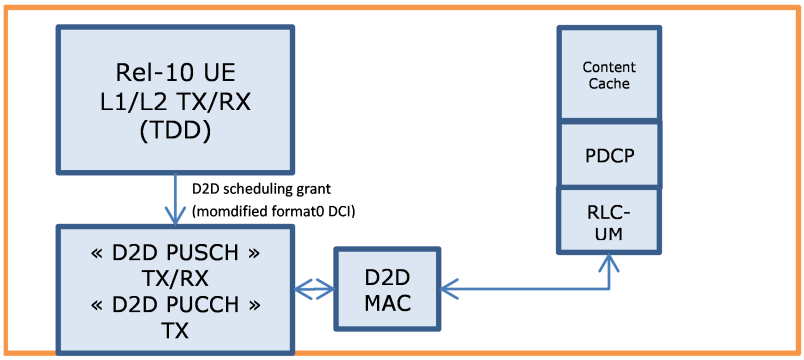


**Figure 5: D2D UE Architecture**

### 2.1.3 Conclusion and next steps

We have proposed two demonstration scenarios covering eMBMS relaying and D2D transmission. The first scenario corresponds to the case of a macro-cell eMBMS transmission with a multi-relay network to extend coverage in difficult to reach zones. The relays operate either on a secondary component carrier or on an orthogonal MBSFN-area in a region around the relays. The implementation consists of a novel relay-nodes scheme comprising conventional eMBMS UE receivers and eMBMS eNB transmission. We envisage the use of a commercial eNB and commercial end-user UEs at the extremities of the network in order to show the realism of the implementation. The second scenario consists of extensions to a conventional UE architecture for D2D transmission. We focus on intra-EUTRAN D2D transmissions reusing the uplink carrier frequency. The target architecture employs TDD framing and both broadcast and scheduled D2D transmission are considered. The latter focuses on application scenarios for relaying of cached content in terminals to their proximity.

For the eMBMS relaying scenario, integration of the relays will begin in Q2 2015 and testing in Q3 2015 using ExpressMIMO2 hardware. Basic eMBMS interoperability testing will be completed with a commercial UE in Q2 2015. Work has begun on precise specification of the D2D extensions within the OAI framework and will be followed by implementation in the OAI UE starting in Q3 2015. The broadcast scenario will be considered first since it is similar to the eMBMS relaying case and does not require adaptations in the eNB.

## 2.2 Use-case 2: Interference Aware receiver for DL MU-MIMO CoMP

### 2.2.1 Selection of algorithm

CoMP (Cooperative Multi-Point), and MU-MIMO (Multi-User MIMO), were introduced in LTE-A in order to improve cell edge user quality of service and to increase cell spectrum efficiency. However, we have shown in deliverable D3.2 [19] that without an interference rejection capability at the receiver, downlink performance would be unacceptable at the UE side. In deliverable D3.2 [19], we considered and evaluated different algorithms in this field. These algorithms have been classified into three categories: Interference Suppression (IS), Maximum Likelihood (ML), and Interference Cancellation (IC) receivers.

A real-time hardware in the loop demonstrator will validate the CoMP concept, combining multi-user MIMO at the base stations with an interference cancellation scheme at the mobile side. The main objective will be to evaluate implementation of these innovative algorithms on the mobile side, while base station signals will be generated by simulation tools. Criteria for evaluation include hardware performance and implementation complexity [1].

Single Layer Minimum Mean Square Error (SL-MMSE) and Interference Aware Maximum Likelihood (IA-ML) have been considered for implementation as on the one hand SL-MMSE seems less complex to implement and on the other hand IA-ML provides the best level of performance of the studied algorithms [19]

A preliminary complexity evaluation of these algorithms (SL-MMSE and IA-ML) has been performed. Complexity has been evaluated in terms of number of real additions and number of real multiplications, number of receive and transmit antennas and number of interferers. For sake of simplicity, received signal and interferer signals are assumed to use the same modulation. For a fair comparison between SL-MMSE and IA-ML, Log Likelihood Ratios (LLR) computations (used as inputs to the Viterbi decoder) have been also taken into account in SL-MMSE complexity calculations.

#### *2.2.1.1 Scenario Description*

We first recall the scenario described in [19]

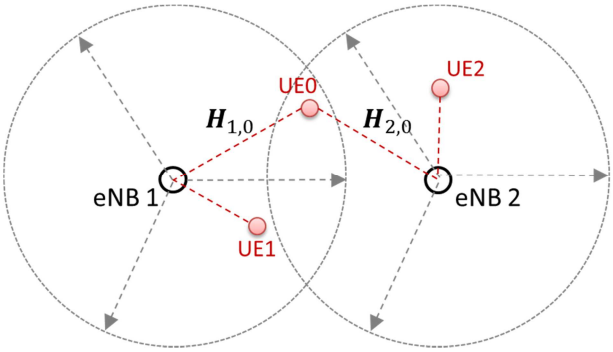


**Figure 6: Scenario of CoMP and MU-MIMO creating interference at the CoMP UE receiver**

As described in Figure 6, the UE of interest is UE0. UE1 is associated to eNB1 whereas UE2 is associated to eNB2. UE1 and UE2 are scheduled on the same time and frequency resource as UE0. UE0 benefits from the cooperation of both eNBs in Joint Processing/Joint Transmission (JP/JT) mode [18][20]. MU-MIMO Transmission Mode 5 (TM5), [22], is used with precoders defined by 3GPP in [21].

The following notations apply:

- $N_R$ is the number of receive antennas (at the UE side),
- $N_T$ is the number of transmit antennas (at the eNB side),
- $N$ is the number of interferers ($N$ =1 or 2)
- $\boldsymbol{H}_{i,0} \in \mathbb{C}^{N_R \times N_T}, i \in \{1,2\}$ is the channel from eNBi to UE0,
- $\boldsymbol{w}_{i,j} \in \mathbb{C}^{N_T \times 1}, i \in \{1,2\}, j \in \{0,1,2\}$ is the precoder applied at eNBi for UEj,
- $x_i \in \mathbb{C}, i \in \{0,1,2\}$ are the data intended to UEi,
- $\boldsymbol{y} \in \mathbb{C}^{N_R \times 1}$ is the signal received at UE0,

- $\boldsymbol{z} \in \mathbb{C}^{N_R \times 1}$ is AWGN with variance $N_0$.

The signal received at UE0 can then be written as in (2.1).

$$\boldsymbol{y} = \boldsymbol{H}_{1,0}\left(\boldsymbol{w}_{1,1}x_1 + \boldsymbol{w}_{1,0}x_0\right) + \boldsymbol{H}_{2,0}\left(\boldsymbol{w}_{2,2}x_2 + \boldsymbol{w}_{2,0}x_0\right) + \boldsymbol{z} \tag{2.1}$$

In order to highlight the interference term, (2.1) can be re-written as in (2.2). Here, the interference is represented by the second sum.

$$\boldsymbol{y} = x_0 \sum_{i=1}^{2} \boldsymbol{H}_{i,0}\boldsymbol{w}_{i,0} + \sum_{i=1}^{2} \boldsymbol{H}_{i,0}\boldsymbol{w}_{i,i}x_i + \boldsymbol{z} \tag{2.2}$$

#### *2.2.1.2 Complexity of SL-MMSE*

The effective channel $\boldsymbol{g}_e$ and interference channels $\boldsymbol{g}_i, i \in \{1,2\}$, are defined in (2.3) and (2.4), by applying the precoders corresponding respectively to UE0, UE1 and UE2 to the MIMO channels $\boldsymbol{H}_{i,0}$ i=1,2.

$$\boldsymbol{g}_e = \sum_{i=1}^{2} \boldsymbol{H}_{i,0}\,\boldsymbol{w}_{i,0} \;\in \mathbb{C}^{N_R \times 1} \tag{2.3}$$

$$\boldsymbol{g}_i = \boldsymbol{H}_{i,0}\boldsymbol{w}_{i,i} \;\in \mathbb{C}^{N_R \times 1}, i \in \{1,2\} \tag{2.4}$$

The Single Layer (SL)-MMSE receiver filter $\boldsymbol{b}$ minimizes the mean square error $e$ w.r.t. the desired signal $x_0$. With perfect knowledge of (2.3) and (2.4), the SL-MMSE receiver can be expressed as:

$$\begin{aligned} e &= E\{\|\boldsymbol{b}^H\boldsymbol{y} - x_0\|^2\} \\ &= \left(\boldsymbol{b}^H - E_x\boldsymbol{g}_e^H\boldsymbol{R}_{\boldsymbol{y}}^{-1}\right)\boldsymbol{R}_{\boldsymbol{y}}\left(\boldsymbol{b}^H - E_x\boldsymbol{g}_e^H\boldsymbol{R}_{\boldsymbol{y}}^{-1}\right)^H + E_x\left(1 - E_x\boldsymbol{g}_e^H\boldsymbol{R}_{\boldsymbol{y}}^{-1}\boldsymbol{g}_e\right) \end{aligned} \tag{2.5}$$

with $E_x$ the transmit signal energy, $\boldsymbol{R}_{\boldsymbol{y}} \in \mathbb{C}^{N_R \times N_R}$ the covariance matrix of the receive signal vector given by (2.6), $\boldsymbol{R}_{\boldsymbol{\eta}} \in \mathbb{C}^{N_R \times N_R}$ the covariance matrix of interference and noise vectors, given by (2.7) and $\boldsymbol{I}_{N_R}$ the identity matrix of size $\boldsymbol{N_R} \times \boldsymbol{N_R}$.

$$\boldsymbol{R}_{\boldsymbol{y}} = E_x\boldsymbol{g}_e\boldsymbol{g}_e^H + \boldsymbol{R}_{\boldsymbol{\eta}} \tag{2.6}$$

$$\boldsymbol{R}_{\boldsymbol{\eta}} = E_x\sum_{i=1}^{2} \boldsymbol{g}_i\boldsymbol{g}_i^H + N_0\boldsymbol{I}_{N_R} \tag{2.7}$$

Finally, the minimum value of (2.5) is obtained for:

$$\boldsymbol{b}^H = \boldsymbol{b}_{SL-MMSE}{}^H = E_x\boldsymbol{g}_e^H\boldsymbol{R}_{\boldsymbol{y}}^{-1} \tag{2.8}$$

The complexity evaluation of SL- MMSE can thus be decomposed in three steps:

1. Complexity evaluation of the calculation of $\boldsymbol{R}_{\boldsymbol{y}}$
2. Complexity evaluation of the calculation of $\boldsymbol{b}_{SL-MMSE}$
3. Complexity evaluation of the calculation of the LLRs (inputs to the Viterbi decoder)

We will consider $\boldsymbol{g}_e$ and $\boldsymbol{g}_i$ i=1,2 and $N_0$ as inputs, since they could be estimated directly using DM-RS. A variant where $\boldsymbol{g}_e$ and $\boldsymbol{g}_i$ i=1,2 are obtained as the product of the $\boldsymbol{N_R}$x$\boldsymbol{N_T}$ MIMO channel matrices $\boldsymbol{H}_{i,0}$ i=1,2 by the respective precoders $\boldsymbol{w}_{i,j} \in \mathbb{C}^{N_T \times 1}, i \in \{1,2\}, j \in \{0,1,2\}$ will also be evaluated.
In addition, for sake of simplicity, we assume $E_x = 1$
We will consider separately the cases $\boldsymbol{N_R}$=2 and $\boldsymbol{N_R}$>2, because for $\boldsymbol{N_R}$=2, the inversion of $\boldsymbol{R}_{\boldsymbol{y}}$ is computationally simple. Also, for SL-MMSE, it is well-known that with 2 antennas, it is possible only to reject 1 interferer. So in this latter case, $\boldsymbol{N}$=1
Note that the following complexity calculations are to be understood **per subcarrier.**

**$N_R$=2**

1. **Step1** Calculation of $\boldsymbol{R_y}$: complexity 16 real multiplications + 14 real additions
2. **Step 2** calculation of $\boldsymbol{b} = \boldsymbol{b}_{SL-MMSE}$: First, compute $\boldsymbol{R_y^{-1}}$ ; since $\boldsymbol{R_y}$ is a 2x2 matrix, its inverse comes at no cost (permutations and change of sign), except for the computation of the matrix determinant (3 real multiplications+ 2 real additions). The "numerator" of $\boldsymbol{R_y^{-1}}$ is then multiplied by the channel vector $\boldsymbol{g_e^{H,}}$ (12 real multiplications and 8 real additions). Then the determinant is inverted (via a look-up table) and multiplied by the "numerator" of $\boldsymbol{g_e^H R_y^{-1}}$ (4 real multiplications). In total: 19 real multiplications and 10 real additions)
3. **Step3**: LLR:

   It is shown in Annex A that LLRs for a QPSK modulation with Gray code are given by

$$\left(\sqrt{2}\,\frac{\boldsymbol{b^H g_e}}{\|\boldsymbol{b}\|^2 \boldsymbol{N_0}}\right) * \boldsymbol{Re}(\boldsymbol{b}^H \boldsymbol{y}) \quad \text{and} \quad \left(\sqrt{2}\,\frac{\boldsymbol{b^H g_e}}{\|\boldsymbol{b}\|^2 \boldsymbol{N_0}}\right) * \boldsymbol{Im}\left(\boldsymbol{b}^H \boldsymbol{y}\right) \qquad (2.9)$$

   So, we must first calculate $\sqrt{2}\,\frac{\boldsymbol{b^H g_e}}{\|\boldsymbol{b}\|^2 \boldsymbol{N_0}}$ . As recalled in Annex A, $\boldsymbol{b^H g_e}$ is real, the complexity is thus 11 real multiplications and 6 real additions. Note that the division is carried out via a look-up table..
   Lastly, two multiplications of $\sqrt{2}\,\frac{\boldsymbol{b^H g_e}}{\|\boldsymbol{b}\|^2 \boldsymbol{N_0}}$ resp. by $\boldsymbol{Re}(\boldsymbol{b}^H \boldsymbol{y})$ and $\boldsymbol{Im}(\boldsymbol{b}^H \boldsymbol{y})$) must be carried out for each symbol.

In case the channel estimation is performed using the $\mathbf{N_R}$x$\boldsymbol{N_T}$ MIMO channel matrices and their multiplication by the respective precoders, we have to add:

- For $\boldsymbol{g}_e$ as given in (2.3), the complexity is: 8 $\boldsymbol{N_R} * \boldsymbol{N_T}$ real multiplications and $\boldsymbol{N_R}$ (4 $\boldsymbol{N_T}$ +2) real additions, so here, 16 $\boldsymbol{N_T}$ real multiplications and 4 (2 $\boldsymbol{N_T}$ +1) real additions
- For $\boldsymbol{g}_i$ i=1 or 2 as given in (2.4), the complexity is: 4 $\boldsymbol{N_R} * \boldsymbol{N_T}$ real multiplications and 2 $\boldsymbol{N_R} * \boldsymbol{N_T}$ real additions, thus 8 $\boldsymbol{N_T}$ and 4 $\boldsymbol{N_T}$ real additions.

**$\underline{N_R > 2}$**

$\boldsymbol{N}$ (number of interferers) can now be equal to 1 or 2.

1. **Step1** Calculation of $\boldsymbol{R_y}$**:** complexity is equal to $\mathbf{2}(\boldsymbol{N}+\mathbf{1})\,\boldsymbol{N_R}$ real multiplications + $2(\boldsymbol{N}+1)\,\boldsymbol{N_R}$ real additions for calculating the diagonal elements, plus $(\boldsymbol{N_R}(\boldsymbol{N_R}-\mathbf{1})/\mathbf{2}) * \mathbf{4}(\boldsymbol{N}+\mathbf{1}))$ real multiplications, and $(\boldsymbol{N_R}(\boldsymbol{N_R}-\mathbf{1})/\mathbf{2}) * (\mathbf{4}\boldsymbol{N}+\mathbf{2}))$ real additions for non diagonal elements.
2. **Step 2**: Calculation of $\boldsymbol{b} = \boldsymbol{b}_{SL-MMSE}$**.**There we can assume that to solve the linear system $\boldsymbol{b} = \boldsymbol{g_e^H R_y^{-1}}$**,**
   We can use the Cholesky decomposition of matrix $\boldsymbol{R_y^{-1}}$ . In that case, the complexity of calculation of b is O($\boldsymbol{N_R^3}$ ).
3. **Step 3**: calculation of the LLRs
   Similar to the case $\boldsymbol{N_R} = \mathbf{2}$**,** we must calculate $\sqrt{2}\,\frac{\boldsymbol{b^H g_e}}{\|\boldsymbol{b}\|^2 \boldsymbol{N_0}}$ The complexity is thus $\boldsymbol{4N_R+3}$ real multiplications and $(2\boldsymbol{N_R}-\mathbf{1}) * \mathbf{2}$ real additions.
   Then, for each symbol, $\boldsymbol{b}^H \boldsymbol{y}$ must be calculated, which takes 4 $\boldsymbol{N_R}$ real multiplications and 2$\boldsymbol{N_R}$ +2($\boldsymbol{N_R}$-1) = 4$\boldsymbol{N_R}$ -2 real additions.

   Then, the multiplications by $\boldsymbol{Re}(\boldsymbol{b}^H \boldsymbol{y})$ and $\boldsymbol{Im}(\boldsymbol{b}^H \boldsymbol{y})$ must be taken into account, i.e. 2*(number of symbols) real multiplications

In case the channel estimation is performed using the $\boldsymbol{N_R}$x$\boldsymbol{N_T}$ MIMO channel matrices and their multiplication by the respective precoders, we have to add:

- For $\boldsymbol{g}_e$ as given in (2.3), the complexity is: 8 $\boldsymbol{N_R} * \boldsymbol{N_T}$ real multiplications and $\boldsymbol{N_R}$ (4 $\boldsymbol{N_T}$ +2) real additions

- For $\boldsymbol{g}_i$ i=1,2 as given in (2.4), the complexity is: 4 $\boldsymbol{N_R} * \boldsymbol{N_T}$ real multiplications and 2 $\boldsymbol{N_R} * \boldsymbol{N_T}$ real additions for each vector.

#### *2.2.1.3 Complexity IA-ML:*

**For a single interferer, equal energy alphabets** :
From [19], the IA-ML metric for computation of LLR of each bit of each symbol is given by:

$$\Lambda_b^i(\boldsymbol{y}, c_{k'}) \approx \min_{x_0 \in \mathcal{X}_{0,b}^i} -\{\bar{y}_{0,R}x_{0,R} + \bar{y}_{0,I}x_{0,I} + |\psi_{A,1}||x_{1,R}| + |\psi_{B,1}||x_{1,I}|\} \quad (2.10)$$

with:

- $\mathcal{X}_0$ the symbols of the constellation,
- $(x)_R$ or $x_R$ the real part of $x$, $(x)_I$ or $x_I$ the imaginary part of $x$,
- $\bar{y}_0 = \left(\boldsymbol{H}_{1,0}\boldsymbol{w}_{1,0} + \boldsymbol{H}_{2,0}\boldsymbol{w}_{2,0}\right)^H \boldsymbol{y}$,
- $\psi_{A,1} = \rho_{0,1R}x_{0,R} + \rho_{0,1,I}x_{0,I} - \bar{y}_{1,R}$,
- $\psi_{B,1} = \rho_{0,1,R}x_{0,I} - \rho_{0,1,I}x_{0,R} - \bar{y}_{1,I}$,
- $\rho_{0,1} = \left(\boldsymbol{H}_{1,0}\boldsymbol{w}_{1,0} + \boldsymbol{H}_{2,0}\boldsymbol{w}_{2,0}\right)^H \left(\boldsymbol{H}_{1,0}\boldsymbol{w}_{1,1}\right)$,
- $\bar{y}_1 = \left(\boldsymbol{H}_{1,0}\boldsymbol{w}_{1,1}\right)^H \boldsymbol{y}$.

Considering that the product of the channel estimates by the precoders has already been estimated, the complexity of the above metric is $\boldsymbol{12N_R + 8}$ real multiplications and $\boldsymbol{12N_R + 1}$ real additions, multiplied by the modulation size, for each symbol.

**For two interferers, equal energy alphabets** :
From [19], the IA-ML metric for computation of LLR of each bit of each symbol is given by:

$$\Lambda_b^i(\boldsymbol{y}, c_{k'}) \approx \min_{x_0 \in \mathcal{X}_{0,b}^i,\ x_1 \in \mathcal{X}_1,\ x_2 \in \mathcal{X}_2} \left\{-(\bar{y}_0^* x_0)_R + \psi_{A,1}x_{1,R} + \psi_{B,1}x_{1,I} + \psi_{A,2}x_{2,R} + \psi_{B,2}x_{2,I} + \left(\rho_{1,2}x_1^* x_2\right)_R\right\} \quad (2.11)$$

with:

- $\mathcal{X}_t$ $t \in \{0,1,2\}$, the symbols of the constellation,
- $\rho_{0,t} = \left(\boldsymbol{H}_{1,0}\boldsymbol{w}_{1,0} + \boldsymbol{H}_{2,0}\boldsymbol{w}_{2,0}\right)^H \left(\boldsymbol{H}_{t,0}\boldsymbol{w}_{t,t}\right),\ t \in \{1,2\}$,
- $\rho_{1,2} = \left(\boldsymbol{H}_{1,0}\boldsymbol{w}_{1,1}\right)^H \left(\boldsymbol{H}_{2,0}\boldsymbol{w}_{2,2}\right)$,
- $\bar{y}_t = \left(\boldsymbol{H}_{t,0}\boldsymbol{w}_{t,t}\right)^H \boldsymbol{y}, \quad t \in \{1,2\}$,
- $\psi_{A,t} = \rho_{0,t,R}x_{0,R} + \rho_{0,t,I}x_{0,I} - \bar{y}_{t,R}, \quad t \in \{1,2\}$,
- $\psi_{B,t} = \rho_{0,t,R}x_{0,I} - \rho_{0,t,I}x_{0,R} - \bar{y}_{t,I}, \quad t \in \{1,2\}$.

Considering that the product of the channel estimates by the precoders has already been estimated, the complexity of the above metric is $\boldsymbol{24N_R + 22}$ multiplications and $\boldsymbol{24N_R + 5}$ additions, multiplied by 3 times the constellation size. for each symbol.

#### *2.2.1.4 Comparison of complexity SL-MMSE vs. IA-ML*

The above complexity calculations are summarized in Table 3. In red, the additional complexity that occurs when channel estimates are computed from the MIMO channel matrices and respective precoders.

**Table 3 Complexity Comparison between SL-MMSE and IA-ML for N=1 or 2 interferers**

| **Receiver Architecture** | **Number of real multiplications** | **Number of real additions** |
|---|---|---|
| **SL-MMSE**<br>QPSK, $\boldsymbol{N_R}$=2, $N$=1 | 46 +10*number of symbols<br>+24 $\boldsymbol{N_T}$ | 30+ 6*number of symbols<br>+ 12 $\boldsymbol{N_T}$ +4 |

| | | |
|---|---|---|
| **Sl MMSE**<br>QPSK, $\underline{N_R}$ >2, $N$ =1 or 2 | O($N_R^3$)+ 2 $N_R^2$ ($N$+1)+ 4 $N_R$ +3+ +(4$N_R$+2)*number of symbols<br>+4$N_{R*}N_T(2+N)$ | $N_R^2$ (2$N$+1) + 4 $N_R$ -2+ (4 $N_R$ - 2)*number of symbols<br>+2$N_{R*}N_T(2+N)$+2 $N_{R*}$ |
| **IA-ML**<br>$N$ =1 | (12$\underline{N_R}$+8)* constellation size (4 for QPSK)* 2*number of symbols<br>+12 $N_{R*}N_T$ | (12$\underline{N_R}$+8)* constellation size*2*number of symbols<br>+6 $N_{R*}N_T$+2 $N_{R*}$ |
| **IA-ML**<br>$N$ =2 | $\underline{(24N_R+22)}$ *3 *constellation size*2*number of symbols<br>+ 16 $N_{R*}N_T$ | $\underline{(24N_R+5)}$ 3* constellation size*2*number of symbols<br>+ 8 $\underline{N_{R*}N_T}$+2 $N_{R*}$ |

Note that the number of symbols can be taken as the number of symbols where the channel, and thus the equalizer, can be considered as constant.

In Figure 7 (resp. Figure 8), complexity in terms of number of multiplications is plotted vs. number of symbols, for $N_{R*}=2$ (resp. $N_{R*}=4$) . The dotted lines refer to the case when channel coefficients are computed from the MIMO channel matrices (figures in red in Table 3)

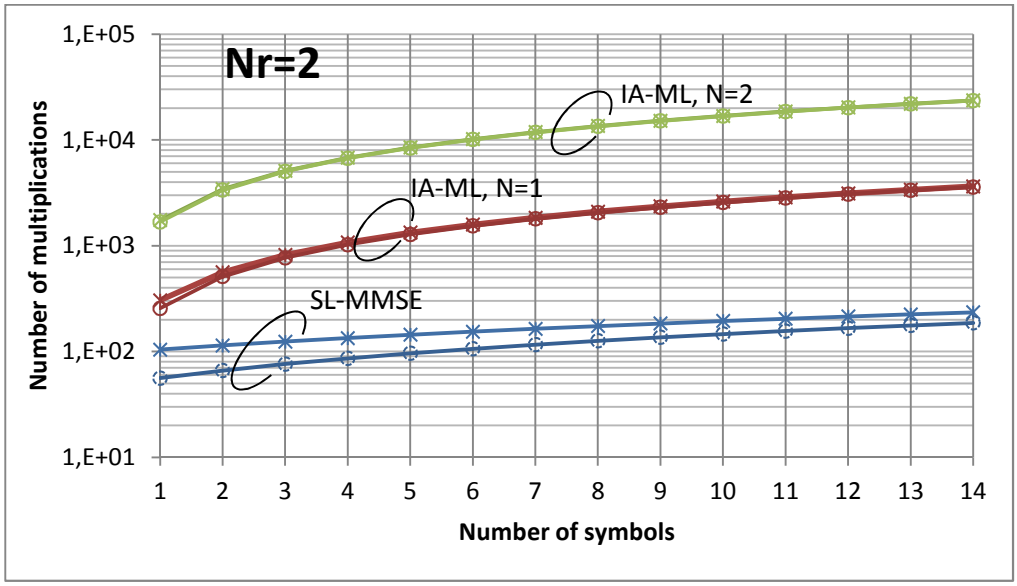


**Figure 7 Comparison of the complexity in terms of number of multiplications between SL-MMSE and IA-ML. Circles**: direct channel vector estimation, **Crosses**: channel vector estimated via the MIMO channel matrix and precoder**.** $\underline{N_{R*}=2}$

We can see on Figure 7 that for QPSK and one symbol, the complexity in terms of real multiplications is multiplied by 4.6 in the case of IA-ML in comparison to SL-MMSE when one interferer is considered. The two interferers case can be only dealt with by IA-ML.

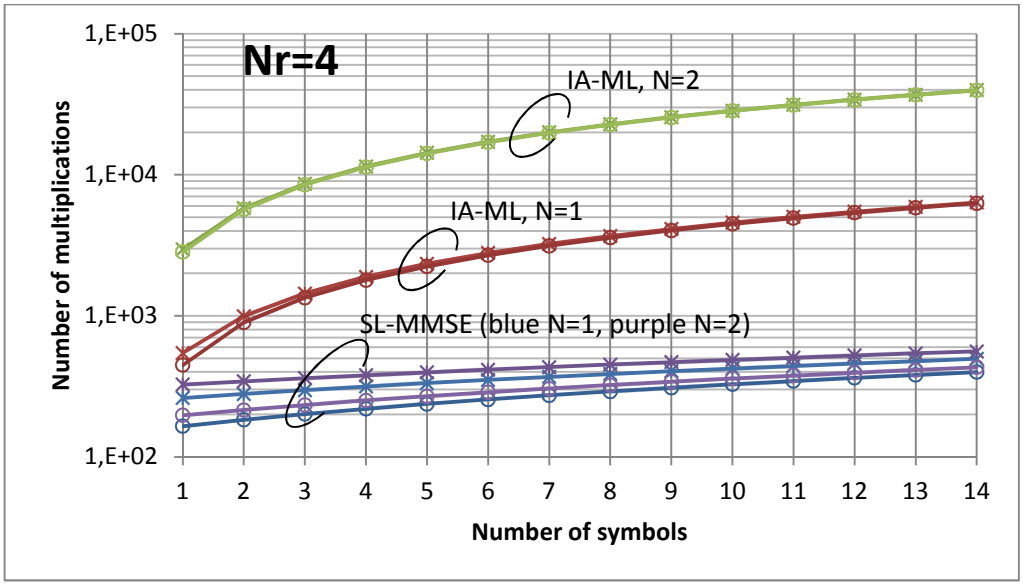


**Figure 8 Comparison of the complexity in terms of number of multiplications between SL-MMSE and IA-ML, Circles**: direct channel vector estimation, **Crosses**: channel vector estimated via the MIMO channel matrix and precoder $N_{B*} = 4$.

We can see in Figure 8 that for QPSK, the complexity in terms of real multiplications for one symbol is multiplied by 15 in the case of IA-ML in comparison to SL-MMSE when one interferer is considered. Furthermore, when two interferers are considered the overhead of complexity is almost equal to 92 between IA-ML and SL-MMSE.

### 2.2.2 Platform implementation

The platform considered for implementation of the DL-MIMO CoMP has been described in [1]. Preliminary implementation and early implementation complexity for SL-MMSE and IA-ML have been considered. Implementation complexity is evaluated in terms of resource usage on the proposed implementation platform that is based around a Xilinx Kintex-7 FPGA. As the algorithms implemented in [19] would be too costly to implement using floating point arithmetics on the physical Kintex-7 platform, finite register dimension impact should be considered. The estimation of the finite register dimension is therefore a prerequisite for resource usage estimation.

#### *2.2.2.1 Finite register estimation*

Finite precision arithmetic used in real-time implementation uses a fixed point representation based on a two's complement representation. A signed physical value, w is considered to be represented by a N-bit integer $a_{N-1}$, $a_{N-2}$, .., $a_0$. The weight of each bit is a power of two, except for the most significant bit, whose weight is the negative of the corresponding power of two.

$$w = -a_{N-1}2^{N-1+LSB} + \sum_{i=0}^{i=N-2} a_i 2^{i+LSB}$$

Where LSB (Lease Significant Bit) is an integer value and N the number of bits used in the finite register representation of w.

This representation can be rewritten as:

$$w = -b_s 2^{MSB+1} + \sum_{i=LSB}^{i=MSB} b_i 2^i$$

Where N = MSB-LSB+2, and the vector [$b_s$, $b_{MSB}$, … $b_{LSB}$] is identical to [$a_{N-1}$, $a_{N-2}$, .., $a_0$]. The notation s[MSB:LSB] can then be used to define the finite register physical representation of the entity w. Using this notation, the quantization step is thus equal to $2^{LSB}$ and the w can represent any value between $-2^{MSB+1}$ and $2^{MSB}-2^{LSB}$ with such a quantization step. This notation will be used in the following of the document for quantized numbers.

We propose in this section to investigate quantization requirements of SL-MMSE and IA-ML for various scenarios in order to define a finite register dimension for implementation.

First, the MU-MIMO case without CoMP has been considered for two users, UE1 and UE2 (see Figure 9).


**Figure 9 MU-MIMO, no CoMP use case**

The cumulative density function of the channel seen at the receiver (after path loss) and of the received data (in the frequency domain) is then estimated. Two scenarios have been considered: distances between UE0 and eNB of 100m and 300m. This corresponds to SNR values of 20dB and 0dB respectively. The results are given in Figure 10 and Figure 11. This corresponds to the most critical interval of usage where the finite register dimension will impact the performance of the system.

The channel model used in the simulations is Spatial Channel Model (SCM) [23].

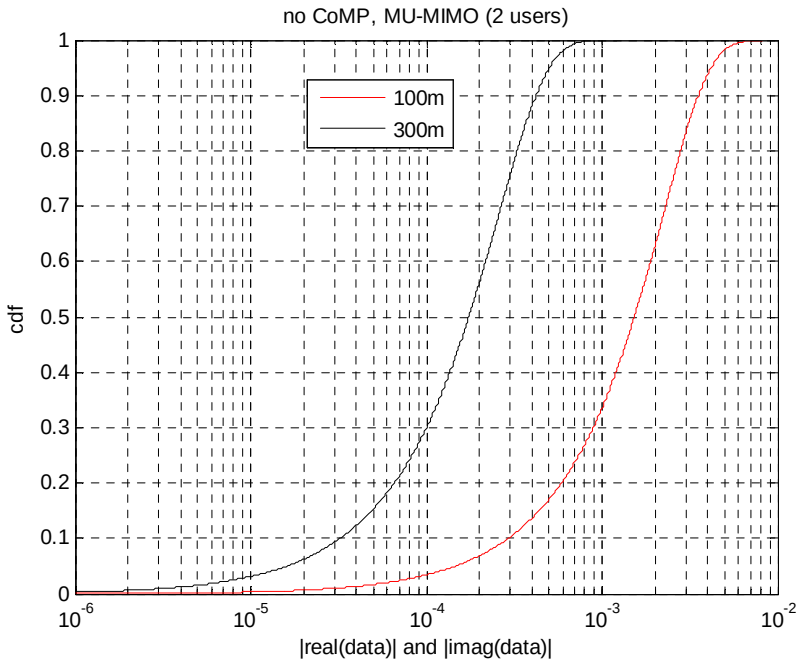


**Figure 10 MU-MIMO, no CoMP – Cumulative density function of received data**

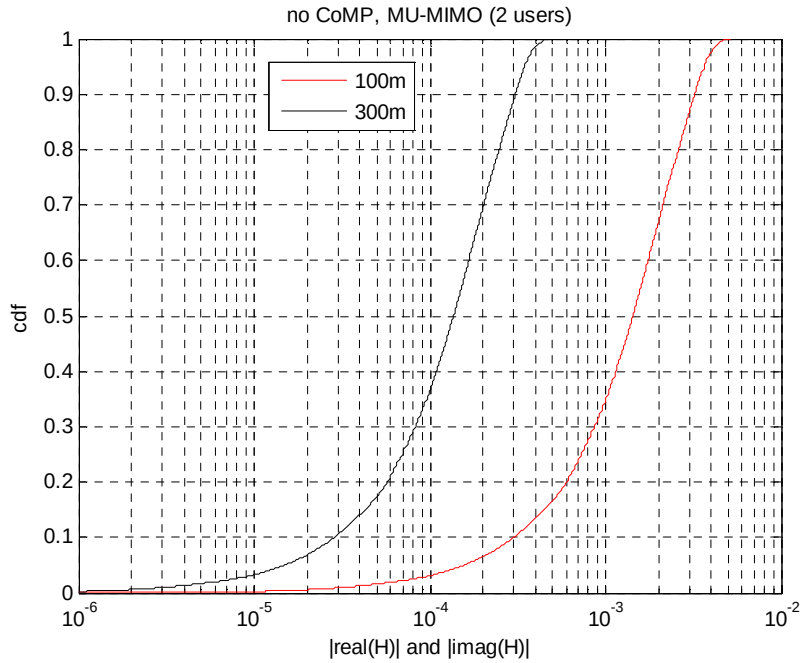


**Figure 11 MU-MIMO, no CoMP – Cumulative density function of received channel**

When UE0 is located at 100 m from the eNodeB, received data level is smaller than $10^{-2}$, while channel coefficients are less than $6.10^{-3}$. Similarly when UE0 is located at 300m from the eNodeB, received data level is less than $10^{-3}$ and channel coefficients are less than 5. $10^{-4}$ assuming a transmit power of 1. This information is useful to evaluate the MSB for this scenario.

Quantization noise is then added to the received channel and data to measure the impact of quantization noise versus Signal-to-Noise Ratio for both SL-MMSE and IA-ML algorithms. Rounding to the nearest $2^{LSB}$ is used for both data and channel to evaluate the value of LSB.

Channel estimates are rounded to their nearest values and expressed in terms of LSB quantization noise.

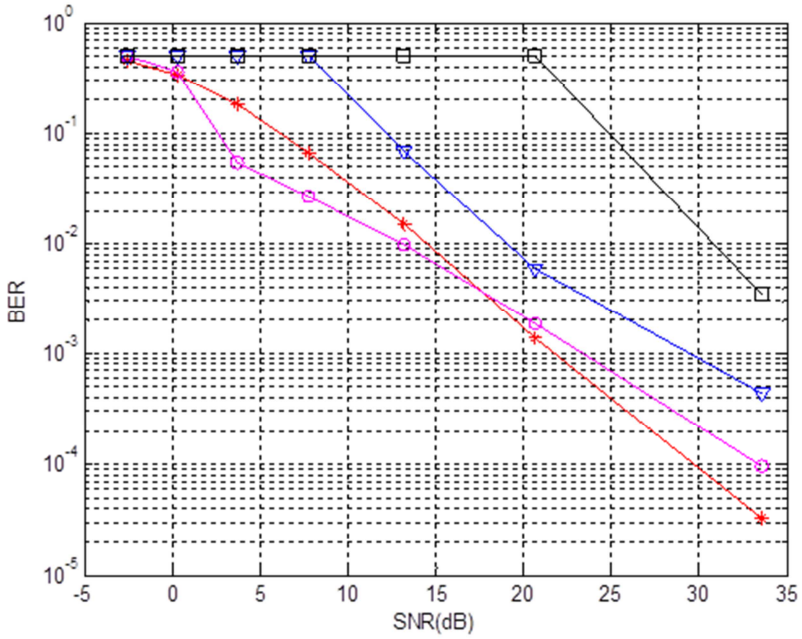


**Figure 12 MU-MIMO, no CoMP – SL-MMSE – BER as a function of quantization noise and SNR**

(Floating point: red, LSB=-11 : magenta, LSB=-9 : blue, LSB=-7 : black)

For SL-MMSE, when channel coefficients are estimated to the nearest $2^{-11}$ level, performance of the algorithm is almost the same as when implemented in floating point (BER target of $10^{-3}$). This suggests that $LSB = -11\ to\ LSB = -10$ is a fair quantization level. Since channel coefficients for target SNR of 20dB, corresponding to a distance of 100 m from eNodeB in these scenarios, are less than $10^{-3}$ , MSB can be set to $\log_2(10^{-3})$-1 or -9. Thus the channel coefficients may be represented on a finite register of representation s[-9:-11] using the previously introduced notation. This is equal to 4 bits

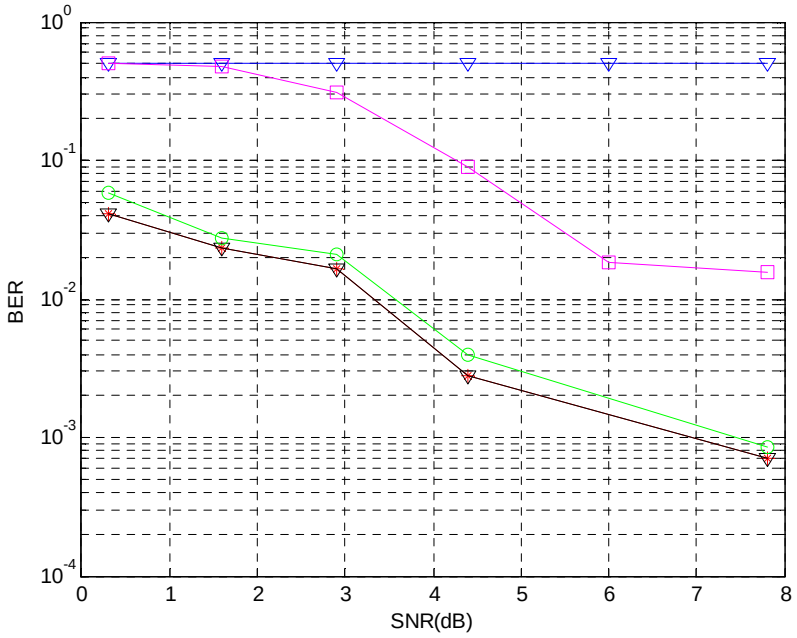


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**Figure 13: MU-MIMO, no CoMP – IA-ML – BER as a function of quantization noise and SNR**

(Floating point: red stars, LSB =-9: blue triangle, LSB= -11: magenta squares, LSB=-13 green circles, LSB=-19 black triangles)

Similarly for IA-ML, quantization level should be in this case at least equal to LSB=-13. As for the same reason channel coefficients are bounded to a MSB of -9, data and channel coefficients should therefore be represented on a finite register of dimension s[-9:-13] or 6 bits.

Then, the MU-MIMO case with CoMP is considered for two users.

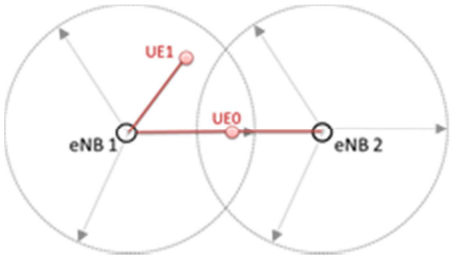



**Figure 14 MU-MIMO, with CoMP**

Similarly cumulative density estimation for data and channel are estimated for both scenarios of UE0 distance from eNB of 100m and 300m. The distance between eNB1 and eNB2 is equal to 500m.

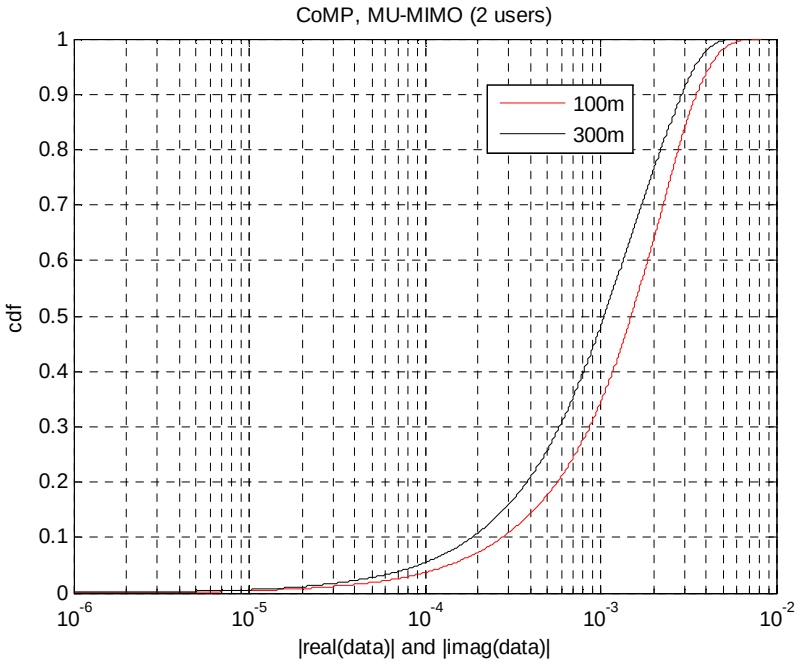



**Figure 15 MU-MIMO, with CoMP – Cumulative density function of received data**

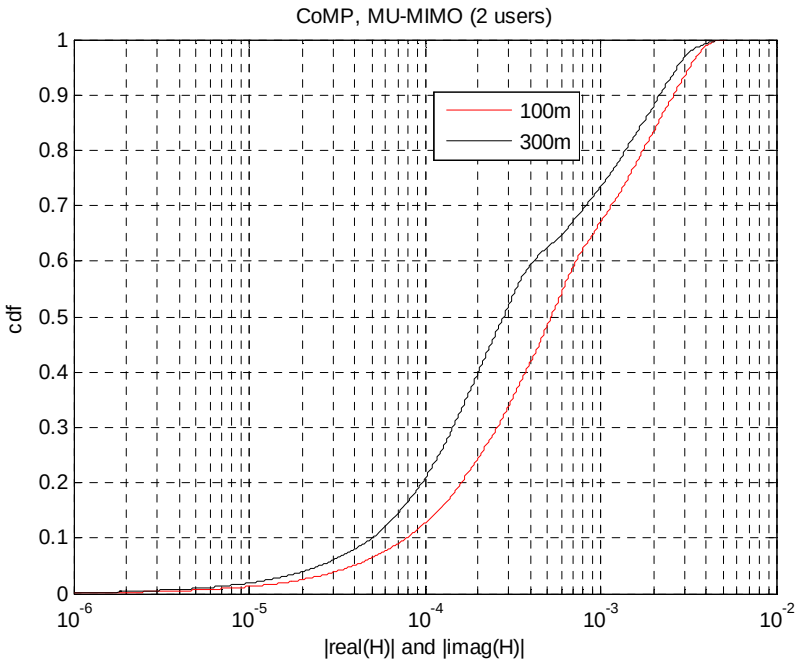



**Figure 16 MU-MIMO, with CoMP – Cumulative density function of received channel**

The distributions are much less dispersive than in the no-CoMP case, since in case 1. UE0 is located at 100m from eNodeB1 and therefore at 400m from eNode2 and for case 2, UE0 is 300m from eNodeB1 but 200m from eNode2. Since our scenario considers that eNode1 and eNode2 have similar transmission properties, this explains that the distributions are much less apart than for the previous scenario. Received data values are less than $8.10^{-3}$ while channel coefficients are less than approximately $5.10^{-3}$.

Similarly to the case without CoMP, performance is then evaluated by adding quantization noise to the received channel. The impact of the quantisation noise as a function of the Signal-to-Noise Ratio for both SL-MMSE and IA-ML algorithms is then estimated.

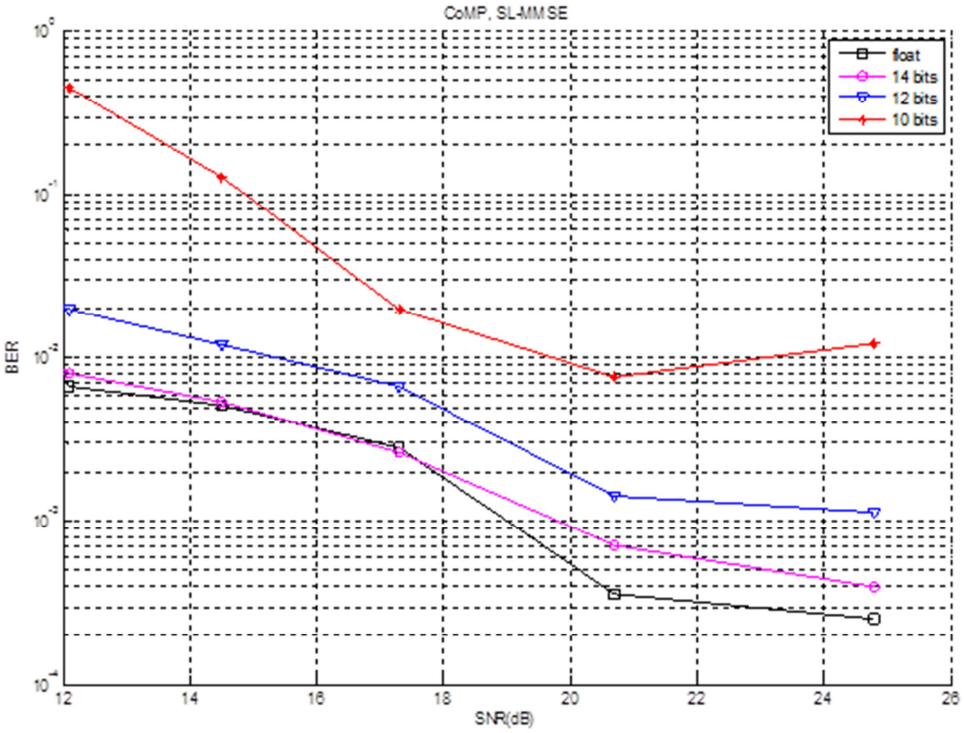



**Figure 17: MU-MIMO, CoMP – SL-MMSE – BER as a function of quantization noise and SNR**

(Floating point : Black, LSB=-9 : Red , LSB=-11 : blue, LSB=-13 : magenta)

Performance of the SL-MMSE algorithm is significantly degraded when quantization noise is above LSB=-13. Since data and channel are less than $8.10^{-3}$ (or $2.10^{-6}$) for these scenarios, we can assume data and channel values may be specified on finite registers of representation s[-6:-13] or on registers of size 9 bits.

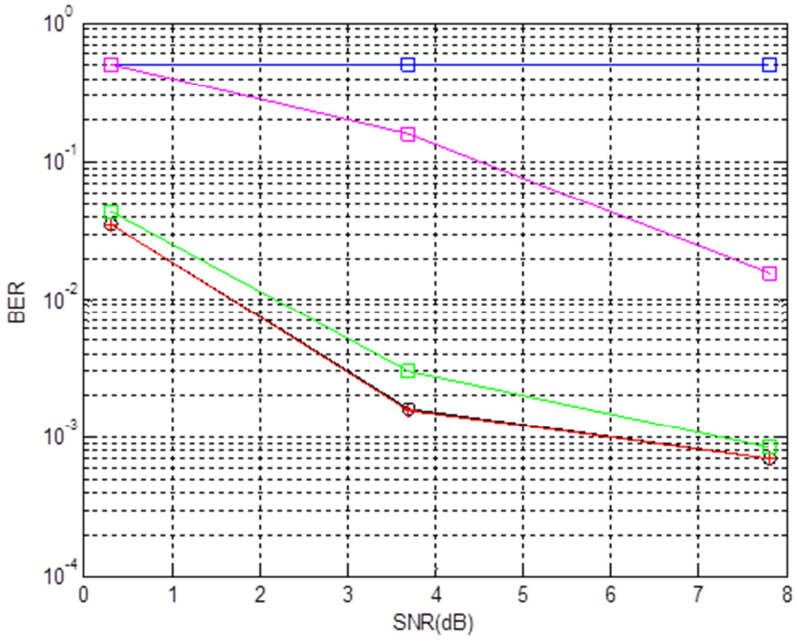



**Figure 18 MU-MIMO, CoMP – IA-ML – BER as a function of quantization noise and SNR**

(Black = Floating point, Red, LSB=-19, Green LSB=-13, magenta LSB=-11, blue LSB=-10)

Performance of the IA-ML algorithm seems to get significantly degraded when quantization noise is above LSB=-13. Since data and channel are less than $8.10^{-3}$ (or $2.10^{-6}$) for these scenarios, we can assume data and channel values may be represented on finite registers of representation s[-6:-13] or on registers of size 9 bits.

We can therefore conclude that a recommended minimum size of finite register for both SL-MMSE and IA-ML algorithm hardware implementation is equal to 9 bits. Both algorithms have eventually been implemented on 12-bits. This takes an internal bit growth of 2 bits into account as well as a contingency of 1 bit for amplitude alignment at the input of the algorithm

The next sections estimate the resources required by the SL-MMSE and IA-ML inside the FPGA using a quantization on 12 bits. An FPGA consists of an array of configurable logic blocks. The logic blocks may be configured and interconnected to implement a function or a design (set of functions). Therefore in order to estimate the cost of an algorithm on an FPGA platform it is useful to estimate the amount of logic blocks the function requires. Four types of resource blocks are usually considered: Slice LUT (lookup tables) implement logic operations such as arithmetic operations, slice registers or flip-flops hold the state of information particularly in the middle of a stream of operations, memory blocks memorize larger amount of information and DSP blocks perform signal processing operations such as multiplications.

The platform used for implementation of the SL-MMSE has been presented in [1] and is based around Kintex-7 XC7325T. This FPGA has the following amount of resources available for algorithm implementation:

**Table 4: Available resources on the Kintex-7 FPGA platform**

| | **Slice LUTs** | **Slice Registers** | **Block RAM** | **DSP** |
|---|---|---|---|---|
| **Kintex-7 XC7325T** | 203800 | 407600 | 445 | 840 |

#### *2.2.2.2 Hardware Implementation of the SL-MMSE algorithm*

As mentioned in Section 2.2.1 the SL-MMSE algorithm was introduced in [19]. It consists in computing one coefficient per receiver antenna for each subcarrier according to the Minimum Mean Square Error criteria. This part of the document will estimate the amount of FPGA resources needed for this algorithm. The resources are the Slice LUTs (logic elements), Slice Registers (flip-flop components) block RAM (memory) and DSP (multipliers, accumulations, …).

The equalization vector is given by the equation (2.8). This equation uses matrix operation. In a system with 2 transmitting antennas and 2 receiving antennas, the matrices maximum size is 2x2. To carry out the computation of the vector, three main parametrizable modules have been designed:

- Conjugate and/or transpose up to 2x2 matrix,
- Up to 2x2 matrix multiplication,
- 2x2 matrix inversion.

The dynamic (integer and decimal part) of each module can be set according to the input power. An output scale factor can be applied to optimize the quantization and get $M \cdot M^{-1} = k \cdot I_d$ where $k$ is a constant value and $I_d$ the identity matrix. The internal quantization of the multipliers input is 18 bits to fit with the maximum dynamic range of the DSP embedded in the FPGA.

The architecture of the SL-MMSE is given in Figure 19. A preliminary architecture based on a fully streamed pipeline architecture has been considered. This provides maximum throughput for the algorithm but may increase implementation cost in terms of required resources.

Let $b^H$ denote the (1,2) equalization filter vector and $y$ the (2,1) received signal vector. The first element references the received signal from the 1st antenna, and the second one the received signal from the 2nd antenna. Thus, the equalized value of user 0 is $\widehat{x_0} = b^H \cdot y$ . The processing requires a (1,2)x(2,1) matrix multiplication. This multiplication requires 10 DSP in Xilinx kintex 7 target.

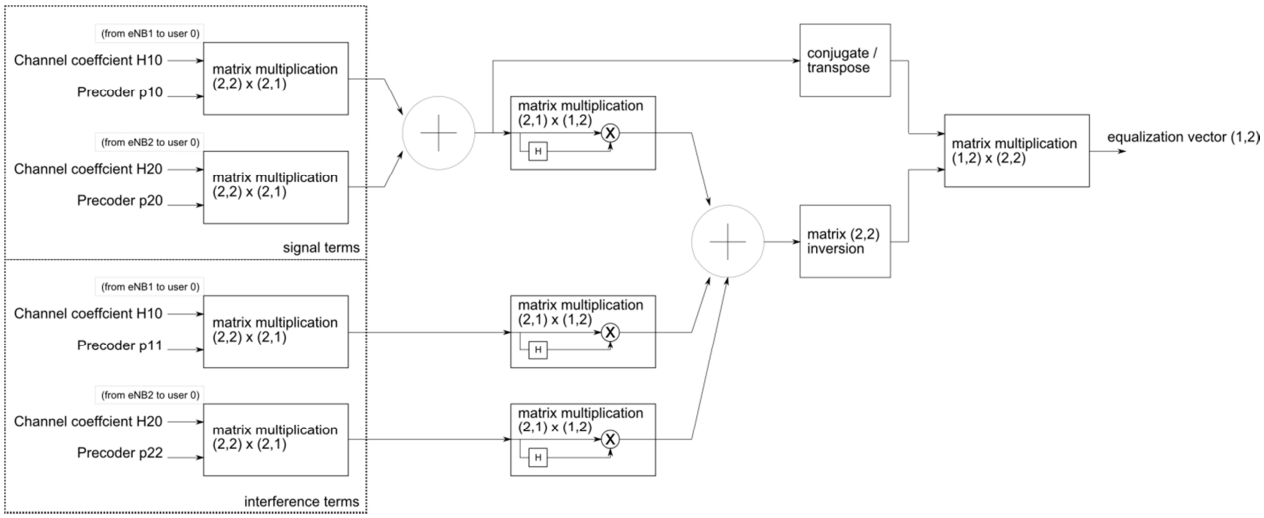



**Figure 19: SL-MMSE estimation architecture**

The study on the input quantization shows that 12 bits can be chosen. The precoder dynamics has been set to 8 bits. The following tables give resource utilization after Xilinx Kintex 7 family mapping. As we can note, the total amount of DSP blocks is smaller than the sum from each separate module (161 vs 167). This may be due to some internal optimisation by the FPGA tool.

.

**Table 5: Resource utilization of the SL-MMSE algorithm**

| | Number of blocks | Slice LUTs | Slice Registers | Block ram | DSP multipliers |
|---|---|---|---|---|---|
| 1st stage multiplier (2,2)x(2,1) | 4 | 379 | 241 | 0 | 20 |
| 2nd stage multiplier (2,1)x(1,2) | 3 | 777 | 881 | 0 | 16 |
| 3rd stage multiplier ((1,2)x(2,2) | 1 | 415 | 257 | 0 | 20 |
| Inversion | 1 | 3129 | 5131 | 3 | 19 |
| SL-MMSE top | 1 | 7460 | 9222 | 6 | 161 |

The same design is depicted in Figure 20, but highlights the multipliers that may be shared. The design can be divided in 3 main matrix multipliers stages and one matrix inversion. Each multiplier of one stage operates on the same input dynamic range.

If we considered a sequential architecture, only one instance of each multiplier is required. Therefore the total amount of DSP is reduced to 56 instead of 148. The state machine to sequence the modules has not been studied as it depends on the data throughput and the design clock frequency.

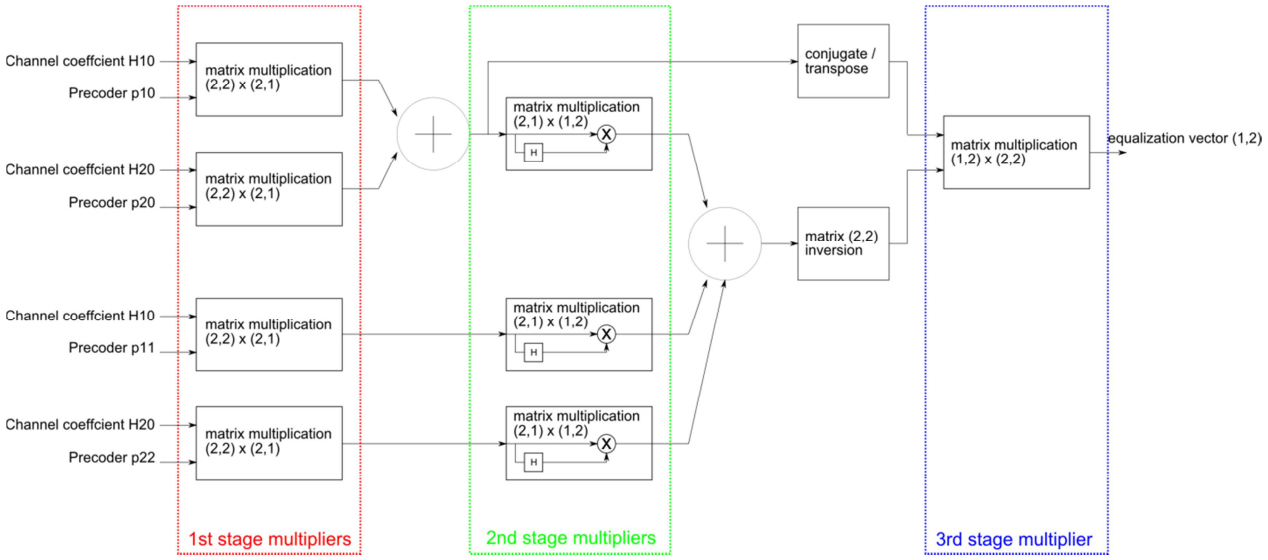



**Figure 20: SL-MMSE estimation architecture with shared multiplier operations highlighted**

#### *2.2.2.3 Hardware Implementation of the IA-ML algorithm*

The IA-ML algorithm was introduced in [19]. It consists in computing the maximum likelihood ratio with the knowledge of the 2 base stations channel matrix. The LLR is composed of two terms, one for the bit equal to 0 and the other for the bit equal to 1. The computation of one term is proposed in Figure 21. The output depends on the x0 alphabet whether the bit is 0 or 1. Thus the LLR is only the difference between these two terms.

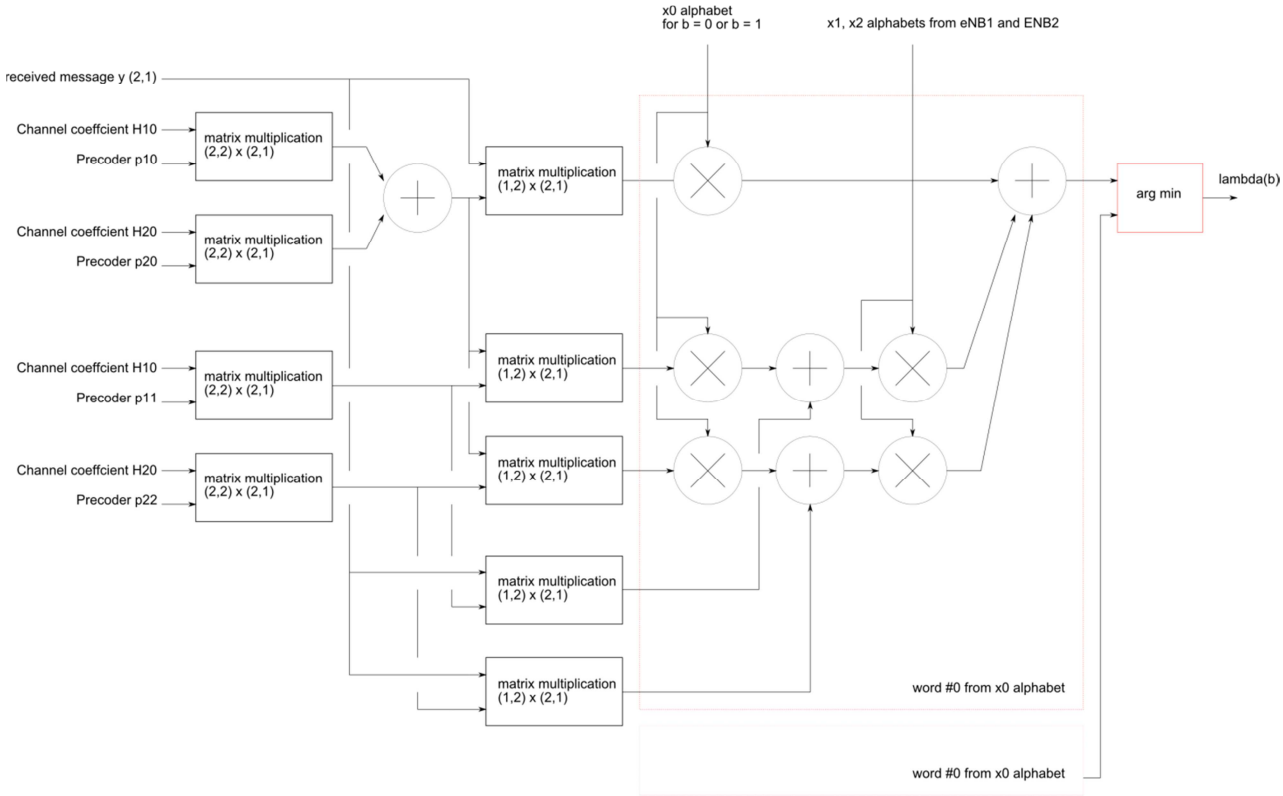



**Figure 21: IA-ML term computation**

The first matrix multiplication stage is the identical to the first stage in SL-MMSE computation (see Figure 19.

The complexity is given in Table 6. As before, the algorithm has been fully pipelined for implementation. The figures given in Table 6 give the partial LLR complexity for one branch. The result has been multiplied by 2 to get the estimate of complexity of the LLR applied to the convolutional decoder. Furthermore, control logic and signal pipeline synchronizations have been omitted and should increase the complexity of the IA-ML algorithm. When control logic and pipeline synchronization is added, estimate of Registers and Block RAM should be similar to the estimates for the SL-MMSE algorithm..

**Table 6: Resource utilization of the IA-ML algorithm (only one term for LLR computation)**

| | **LUTs** | **Registers** | **Block RAM** | **DSP** |
|---|---|---|---|---|
| **IA-ML Branch 1 or 2** | 4600 | 3200 | N/A | 166 |
| **IA-ML Top Estimate** | 9200 | 6400 | N/A | 332 |

#### *2.2.2.4 Complexity Comparison, conclusion and next steps*

Both SL-MMSE and IA-ML resource utilization is then compared to a standard block of a LTE OFDM receiver that is the Fast Fourier Transform (FFT). FFT resource utilization for the LTE 10MHz mode has been estimated in [24]. It is given in Table 7 below and compared to SL-MMSE and IA-ML resource utilization estimates.

**Table 7: Comparison to LTE 10MHz FFT implementation (1024 points)**

| | **LUTs** | **Registers** | **Block RAM** | **DSP** |
|---|---|---|---|---|
| **FFT LTE 10MHz** | 3805 | 5131 | 10 | 13 |
| **SL-MMSE** | 7460 | 9222 | 6 | 161 |
| **IA-ML** | 9200 | 6400 | N/A | 332 |
| **Ratio SL-MMSE/FFT** | 1.96 | 1.8 | 0.6 | 12.4 |
| **Ratio IA-ML/FFT** | 2.4 | 1.3 | N/A | 25.5 |

Logic resource usage is about twice as complex for both algorithms as for the FFT. The same applies to register utilization. It should be noted that IA-ML register utilization has been significantly underestimated and should be similar to SL-MMSE as pipeline synchronization has not been taken into account. However DSP resource usage is significantly increased and is an important dimensioning factor for the implemented algorithms. As much as 12 to 26 times more DSP resources are used by the algorithms than would be used for the FFT algorithm considering the implemented architecture.

**Table 8: Ratio between SL-MMSE and IA-ML resource utilization and Kintex-7 XC7K325T available resources**

| | LUTs | Registers | Block RAM | DSP |
|---|---|---|---|---|
| **XC7K325T** | 203800 | 407600 | 445 | 840 |
| **SL-MMSE** | 7460 | 9222 | 6 | 161 |
| **IA-ML** | 9200 | 6400 | N/A | 332 |
| **Occupation Ratio SL-MMSE** | 3.6% | 2.2% | 1.3% | 19.2% |
| **Occupation Ratio IA-ML** | 4.5% | 1.6% | N/A | 39.5% |

The ratio between the resource utilization and the total amount of available resource in the Kintex-7 FPGA of the demonstration platform is calculated. The result shows once again, that apart from the DSP resources, the algorithm is maps very into the platform.

This suggests that DSP resource sharing should be further investigated to reduce the amount of necessary DSP resources and therefore the cost of implementation of the CoMP algorithm.

## 2.3 Use-case 3: Carrier Aggregation

### 2.3.1 Reconfigurable RF front-end to support carrier aggregation

#### *2.3.1.1 Selection of technology*

The scope of this proof of concept (PoC) is to develop a reconfigurable and flexible bandwidth RF front-end supporting intra-band carrier aggregation (CA) and inter-band CA adjusting the RF output power level according to the CA configuration providing energy savings.

In [2], a reconfigurable power amplifier (PA) for small cell scenarios has been studied to support CA. It is a promising solution to adapt to different CA modes providing energy savings versus a conventional PA. In small cell scenarios, it is reasonable to use a unique PA per various component carriers (CCs) to reduce the size and the cost because the power levels that PA handles are not strongly challenging as in macro cell scenarios.

The PA requirements have been evaluated in order to fulfill 3GPP standard depending on the CA mode and the number of CCs. Firstly, the study has focused on intra-band contiguous CA and it will extend to intra-band non-contiguous CA within WP3. E-UTRA test models [3] were selected to perform the simulations and these signals will be used for PoC validation. Specially, E-UTRA test model 1.1 (E-TM1.1) will verify most of requirements related to the PA.

Several simulations were performed to define the PA requirements depending on the number of CCs for intra-band contiguous CA. The detailed evaluation is included in [2], and Table 9 presents a summary of complementary cumulative distribution function (CCDF)of peak-to-average power ratio (PAPR) and adjacent channel leakage ratio (ACLR) evaluations. Both evaluations were merged to define the PA requirements in order to develop a reconfigurable PA capable of working with up to 5 CCs optimizing energy efficiency. Table 9shows 0.01% CCDF (PAPR) results and PA output back-off (OBO) level to reach 45 dB ACLR depending on the number of contiguous CCs.

**Table 9 PA OBO requirements evaluating 0.01% CCDF (PAPR) and ACLR for different number of CCs (using E-TM1.1)**

| Number of CCs | 0.01% CCDF (PAPR) | PA OBO (ACLR = 45 dB) | Total PA OBO |
|---|---|---|---|
| 1 | 9.6 dB | 8.7 dB | 9.6 dB |
| 2 | 11.8 dB | 13.4 dB | 13.4 dB |
| 3 | 13.3 dB | 15.9 dB | 15.9 dB |
| 4 | 14.3 dB | 17.7 dB | 17.7 dB |
| 5 | 15.2 dB | 18.9 dB | 18.9 dB |

ACLR requirement is more stringent than 0.01% CCDF (PAPR) parameter in all cases except for a single CC. Therefore a unique reconfigurable PA should take into account 9.6 dB OBO level for 1 CC, 13.4 dB for 2 CCs, 15.9 dB for 3 CCs, 17.7 dB for 4 CCs and 18.9 dB for 5 CCs in case of intra-band contiguous CA. The solution proposes reconfigurable operating points at PA to optimize energy efficiency depending on the number of CCs and CA mode.

The PoC demonstrator will evaluate the reconfigurable RF front-end performance for intra-band contiguous CA, intra-band non-contiguous CA and inter-band CA. The main goal will be the assessment of the reconfigurable power amplifier, calculating the power savings versus a conventional power amplifier.

#### *2.3.1.2 Platform implementation*

The PoC demonstrator performs the transmitter of a small cell base station (BS) supporting intra-band CA and inter-band CA. Due to lab equipment constraints, the demonstrator will be limited to a maximum of 3 CCs. Anyway, it would be enough to validate the proposed solution.

For the PoC demonstrator, the average output power per CC has been defined to be15 dBm. Considering that the maximum number of CCs will be 3, the maximum average output power is 19.7 dBm.

Furthermore, according to the analysis performed in WP3 the PA OBO for 3 CCs should be at least 15.9 dB. Therefore the peak output power could be 35.6 dBm. Table 10 summarizes the total output power, the PA OBO and the peak output power for different number of CCs.

**Table 10 Total output power, PA OBO and peak output power depending on the number of CCs**

| Number of CCs | Output power per CC | Total output power | Total PA OBO | Peak output power |
|---|---|---|---|---|
| **1 CC** | 15 dBm | 15 dBm | 9.6 dB | 24.6 dBm |
| **2 CCs** | 15 dBm | 18 dBm | 13.4 dB | 31.4 dBm |
| **3 CCs** | 15 dBm | 19.7 dBm | 15.9 dB | 35.6 dBm |

These PA requirements are the baseline to design the PoC demonstrator. The reconfigurable PA to support up to 3 CCs in intra-band CA configuration should have 1dB compression output power higher than 36-37 dBm. For 1 CC or 2 CCs, the PA requirements lighten and different operating points at PA could reach the PA requirements improving energy efficiency versus a fixed operating point typical in a conventional PA.

In case of inter-band CA, the PA requirements for LTE band 20 will refer only to 1 CC. Therefore the PA should have 1dB compression output power higher than 25-26 dBm. This component could be switched off for intra-band CA configuration.

For experimental validation, LTE band 7 (2620-2690 MHz) was selected to implement intra-band CA and LTE band 7 (2620-2690 MHz) and LTE band 20 (791-821 MHz) for inter-band CA. .Figure 22 shows the proposed block diagram of the CA demonstrator.

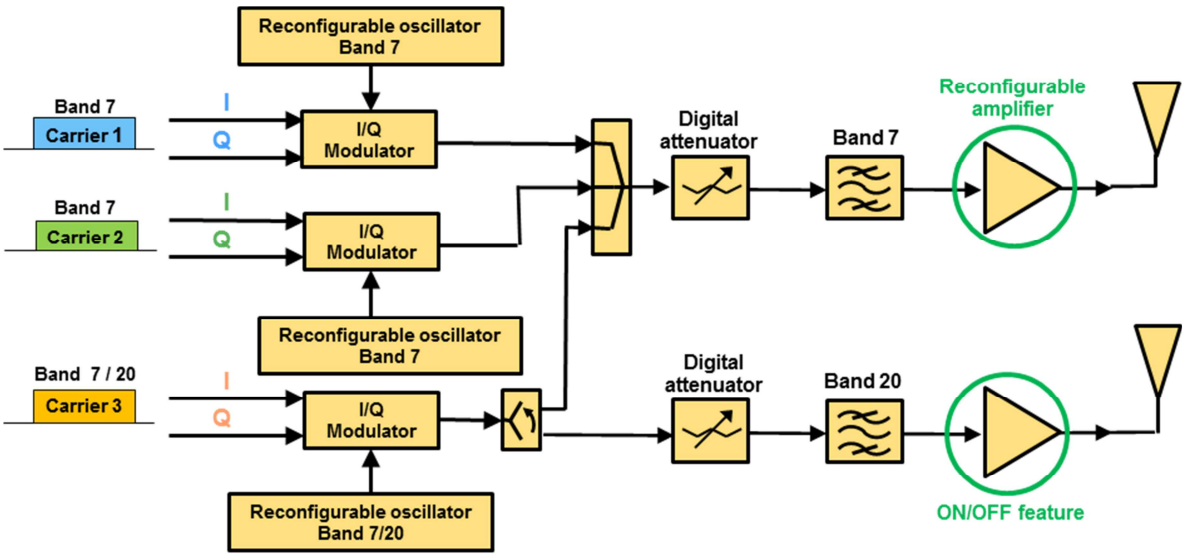



**Figure 22 Block diagram of the CA demonstrator**

There will be up to 3 CCs for intra-band CA in LTE band 7. The first and the second CC will always operate in LTE band 7, while the third CC could operate in LTE band 7 or LTE band 20 to enable inter-band CA.

Input signals will be provided by a signal vector generator such as N5182A together with Signal Studio software N7624B. This software is a flexible suite of signal-creation tools for component and transmitter test. It enables to create waveforms to characterize the power and modulation performance of components and transmitters. Basically, E-UTRA test models (E-TM) will be used during the PoC

validation. The signal vector generator facilitates baseband signals of these E-UTRA test models which will be the input signals for the hardware prototype.

Using a quadrature modulator, the signals will be up converted to RF with the support of a reconfigurable oscillator. Due to lab equipment constraints, only one CC will be generated and duplicated to configure different CA modes. Nevertheless, this restriction won't impact significantly over the results. An RF combiner and an RF switch will be used to build up the different CA modes.

Next in the proposed block diagram, there is a digital attenuator which will enable different output power levels at PA to evaluate its performance. Moreover a bandpass filter at LTE band 7 and LTE band 20 is also introduced to reduce spurious emissions. And finally, the reconfigurable power amplifier is implemented at LTE band 7 consisting in various stages which will be the key point of the evaluation, and a power amplifier at LTE band 20 with ON/OFF features for inter-band CA.

In the following sections, preliminary results of the proposed block diagram are presented showing the progress on the PoC demonstrator.

#### 2.3.1.2.1 Test signals

Using the Signal Studiosoftware N7624B, different test models (E-TM) are available to characterize the power and modulation performance of components and transmitters. A different test model should be selected according to the required test case. In this evaluation focused on the reconfigurable PA performance, the considered test model, E-TM1.1, should be used for tests on:

- BS output power
- Unwanted emissions – Occupied bandwidth, ACLR, operating band unwanted emissions, transmitter spurious emissions
- Transmitter intermodulation
- Reference signals absolute accuracy

Figure 23 shows the measured spectrum using E-TM1.1 signal with 10 MHz bandwidth. In this case without RF impairments, ACLR results are higher than 58 dBc when the ACLR limit is 45 dBc according to 3GPP specifications. This test signal with different bandwidths will be used in most of the validation tests.

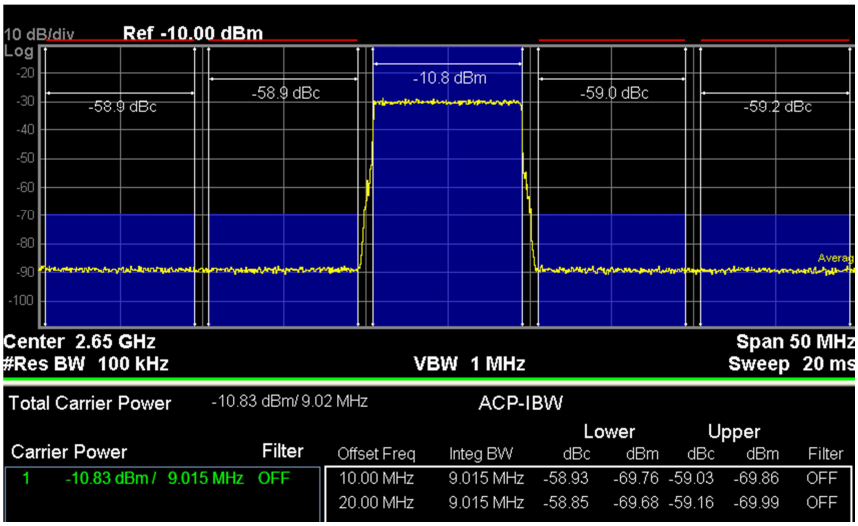



**Figure 23 Measured spectrum using 10MHz ETM1.1 signal**

Figure 24 presents the measured CCDF (PAPR) results for E-TM1.1 signal with 10MHz bandwidth. For 0.01% CCDF, there is a 9.6 dB PAPR and the peak value is 11.6 dB. These values are in line with WP3 simulation results.

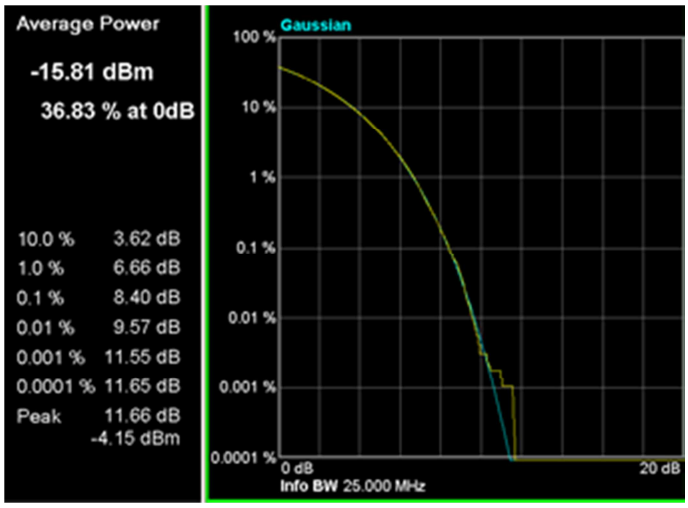



**Figure 24 Measured CCDF (PAPR) results for 10MHz ETM1.1 signal**

#### 2.3.1.2.2 Quadrature modulator

The test model signals in baseband are sent to the quadrature modulator AD8349 from Analog Devices. It is designed for use from 700 MHz to 2700 MHz, therefore it is appropriate to operate at LTE band 20 and LTE band 7.

An evaluation board with 3 quadrature modulators was manufactured. There are two common quadrature input signals (I/Q signals) from the vector signal generator (N5182A) which are split to the 3 quadrature modulators generating 3 CCs to build up the CA configuration. Each quadrature modulator has its dedicated reconfigurable oscillator to define the RF frequency.

Figure 25 shows the evaluation board with the 3 quadrature modulators. There is a buffer at the input to split the input signals (I/Q signals) to the 3 quadrature modulators and each one has an operational amplifier to adjust the baseband input level for the best performance. For baseband signals with high PAPR such as LTE-A, the peak signal should be below the AD8349's compression level in order to prevent clipping of the signal peaks. In the case of LTE-A, clipping results in an increase of signal leakage into adjacent channels. In general, the baseband drive should be at a level where the peak signal power of the output signal is at least a crest factor below the AD8349's output compression point.

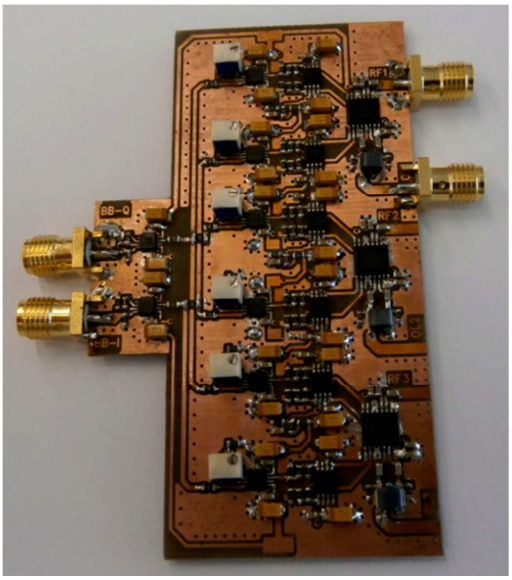


**Figure 25 Evaluation board with the 3 quadrature modulators – AD8349**

Figure 26 presents the output signal of the quadrature modulator, AD8349, using E-TM1.1 signal with 10 MHz bandwidth in LTE band 7 (2.65 GHz). The output signal level is around -16 dBm and ACLR is higher than 54 dBc.

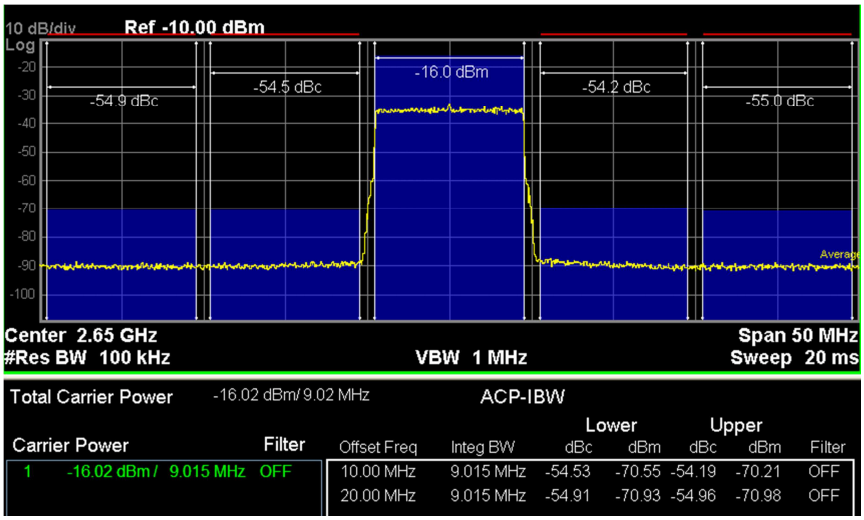



**Figure 26 Measured output signal at quadrature modulator using 10MHz ETM1.1 in LTE band 7 (2.65 GHz)**

For LTE band 20 (800 MHz), the output signal level is around -9 dBm and ACLR is higher than 59 dBc as shown in Figure 27.

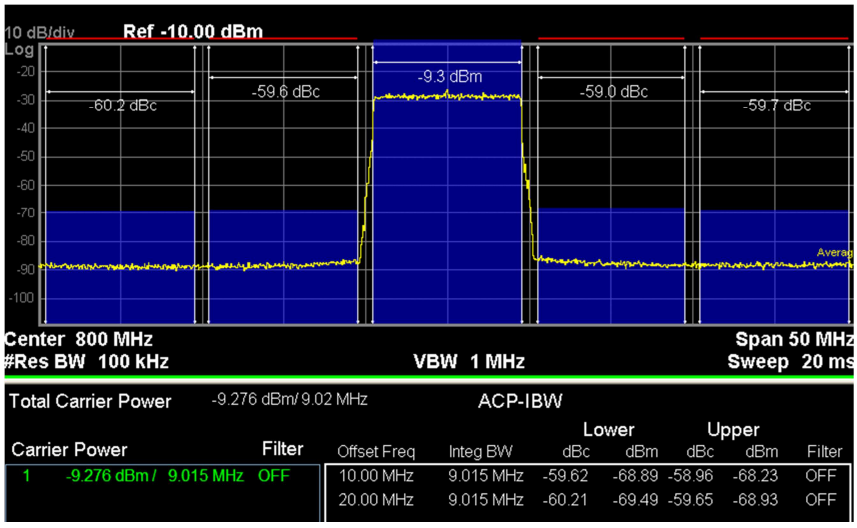



**Figure 27 Measured output signal at quadrature modulator using 10MHz ETM1.1 in LTE band 20 (800 MHz)**

#### 2.3.1.2.3 Reconfigurable oscillators

Three reconfigurable oscillators should be designed, one for each quadrature modulator to enable several CA configurations, intra-band contiguous, intra-band non-contiguous and inter-band CA with different bandwidth and different gaps among CCs. A wideband synthesizer with integrated voltage controlled oscillator (VCO), ADF4350 from Analog Devices was selected. The ADF4350 has an integrated VCO with a fundamental output frequency ranging from 2200 MHz to 4400 MHz. In addition, divide-by-1/2/4/8 or 16 circuits allow the user to generate RF output frequencies as low as 137.5 MHz. Therefore it could generate RF output frequencies in LTE band 20 (791-821 MHz) and LTE band 7 (2620-2690 MHz).Table 11 summarizes the RF frequencies which have been defined for PoC validation in order to enable several CA configurations.

**Table 11 RF frequencies defined for PoCvalidation at LTE band 20 and LTE band 7**

| Band 20 (791-821 MHz) | Band 7 (2620 – 2690 MHz) | |
|---|---|---|
| 796 MHz | 2625 MHz | 2660 MHz |
| 801 MHz | 2630 MHz | 2665 MHz |
| 806 MHz | 2635 MHz | 2670 MHz |
| 811 MHz | 2640 MHz | 2675 MHz |
| 816 MHz | 2645 MHz | 2680 MHz |
| | 2650 MHz | 2685 MHz |
| | 2655 MHz | 2690 MHz |

A high precision TCXO oscillator operating at 10 MHz was selected as input reference in the reconfigurable oscillator design. Figure 28 shows the evaluation board with 3 wideband synthesizers (ADF4350) manufactured.

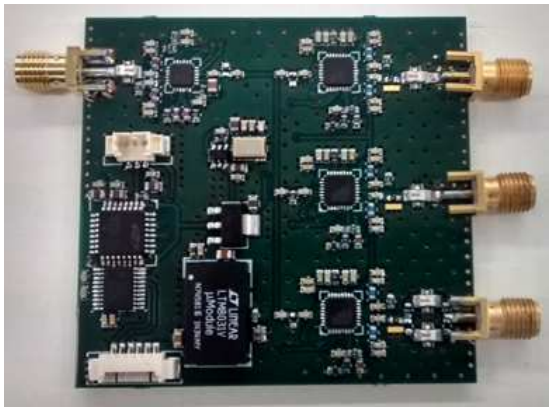
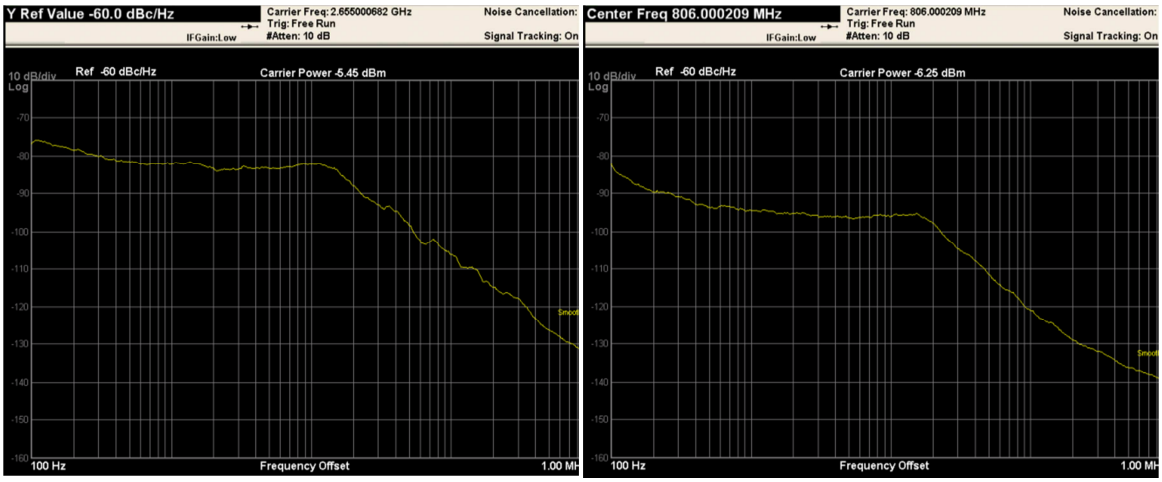


**Figure 28 Evaluation board with 3 wideband synthesizers – ADF4350**

The phase noise performance at LTE band 20 and LTE band 7 was evaluated (Figure 29).




a) b)

**Figure 29 Measured phase noise a) at LTE band 7 and b) LTE band 20**

#### 2.3.1.2.4 Carrier aggregation configuration

To perform different CA configurations, the 3 CCs generated with the quadrature modulators and the reconfigurable oscillators will be combined using RF combiners and RF switches. The first CC will always operate in LTE band 7 representing the baseline configuration. Intra-band contiguous and intra-band non-contiguous CA with 2CCs will be configured adding the second CC using a RF combiner. The reconfigurable oscillators will enable to configure different bandwidths and different gaps between CCs for intra-band non-contiguous CA. The second CC will be also working only in LTE band 7.Finally, the third CC will make possible intra-band CA with 3CCs and inter-band CA, using a RF switch to work in LTE band 20 or in LTE band 7. Figure 30 presents the block diagram to build up the different CA configurations.

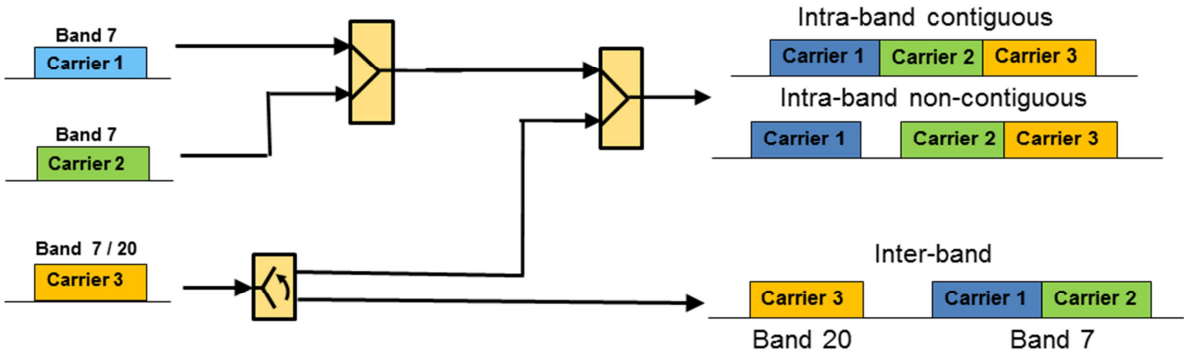



**Figure 30 Block diagram to build up different CA configurations**

TCP-2-272 from Minicircuits is a wideband combiner which operates from 5 to 2700 MHz. Therefore it could combine LTE band 20 and LTE band 7 signals. It presents around 0.9 dB insertion loss. HMC349LP4 from Hittite is a high isolation SPDT non-reflective switch which works from DC to 4 GHz. An evaluation board using TCP-2-272 and HMC349LP4 was done to combine up to 3 CCs and perform different CA configurations (Figure 31).

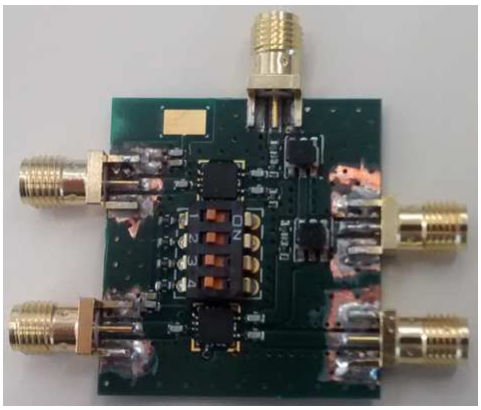


**Figure 31 Evaluation board to combine up to 3CCs to perform different CA configurations (intra-band and inter-band CA)**

#### 2.3.1.2.5 Digital attenuator

To achieve different output power levels at PA and evaluate its performance with different CA configurations, a digital attenuator is introduced. HMC624LP4 from Hittite is a broadband 6-bit GaAs IC digital attenuator whose frequency range is from DC to 6 GHz. Its attenuation range is 31.5 dB with 0.5 dB less significant bit (LSB) step.


**Figure 32 Evaluation board of the digital attenuator – HMC624LP4**

Depending on the CA configuration, different OBO levels will be required as it has been studied in [2]. The digital attenuator will enable these different OBO levels to characterize the reconfigurable PA performance. Figure 33 presents measured insertion loss and output return loss in HMC624LP4 for different attenuation levels.

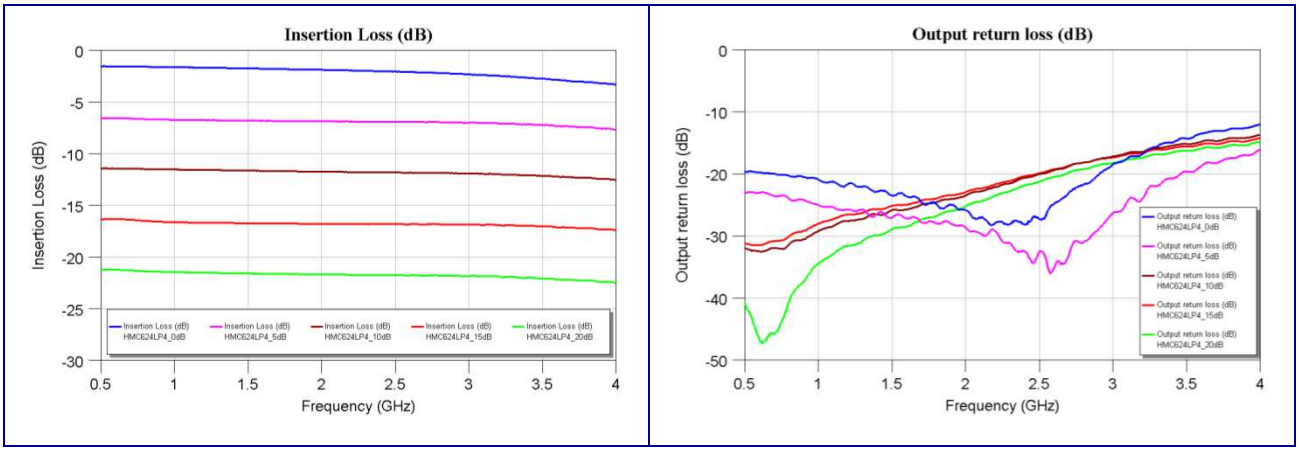



**Figure 33 Measured insertion loss and output return loss from the evaluation board of the digital attenuator for different attenuation levels**

#### 2.3.1.2.6 Reconfigurable power amplifier at LTE band 7

The reconfigurable power amplifier at LTE band 7 consists of three amplifier stages: a pre-driver, a driver and a power amplifier. The pre-driver, ADL5602 from Analog Devices, is a broadband 20dB linear amplifier that operates at frequencies up to 4 GHz. The ADL5602 provides a gain of 20dB, which is stable over frequency, temperature, power supply, and from device to device. The device is internally matched to 50 Ohms at the input and output, making the ADL5602 very easy to implement in a wide variety of applications.

The driver, ALM32220 from Avago Technologies, is a high linearity 2 Watt PA with good 3rd output intermodulation power (OIP3) performance and exceptionally good power added efficiency (PAE) at 1dB gain compression point. It operates from 1.7 GHz to 2.7 GHz. All matching components are fully integrated within the module, which makes it extremely easy to use.

An evaluation board with the pre-driver and the driver amplifier was designed and manufactured for LTE band 7 as shown in Figure 34

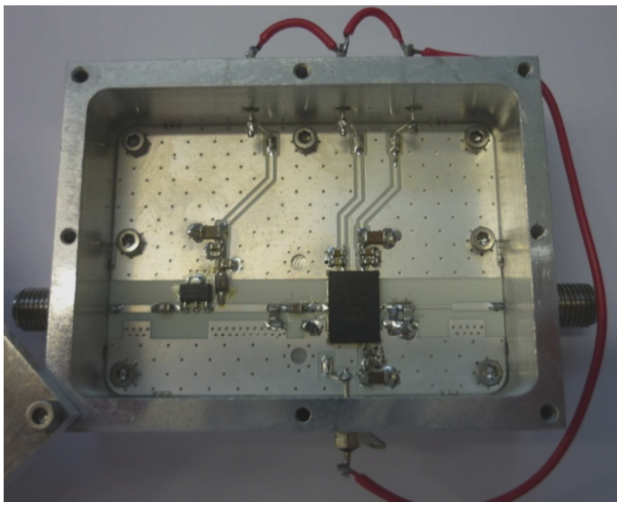


**Figure 34 Evaluation board of the pre-driver and the driver amplifier – ADL5602 and ALM32220**

Figure 35 shows the measured return loss and gain of the evaluation board. The gain at LTE band 7 is around 33 dB and the return loss is higher than -15dB.

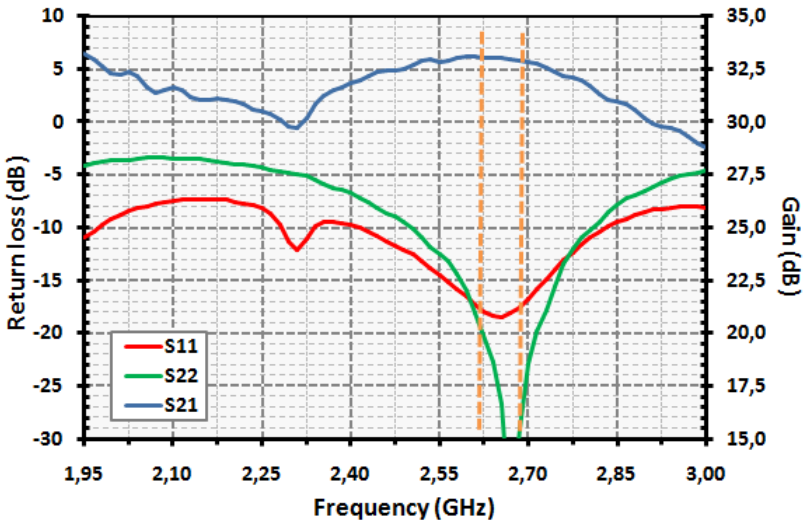



**Figure 35 Measured return loss and gain from the evaluation board – ADL5602 and ALM32220**

In the proposed PoC demonstrator, the average output power per CC has been defined to be 15 dBm. In case of up to 3CCs, the PA OBO should be at least15.9 dB, so the peak output power is 35.6 dBm. Therefore the high power amplifier (HPA) should deliver 1dB compression output power higher than 36-37 dBm. The HPA AFT20S015 from Freescale was selected. It is a LDMOS transistor which covers the frequency range of 1805 to 2700 MHz. An evaluation board designed specifically at LTE band 7 was manufactured (Figure 36).

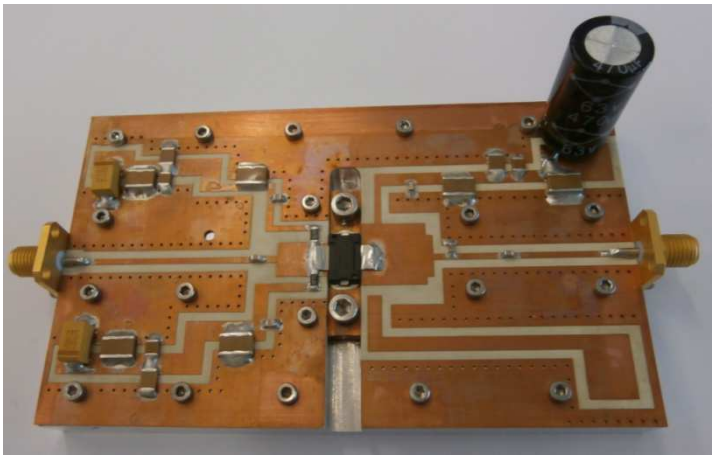


**Figure 36 Evaluation board of the high power amplifier – AFT20S015**

This HPA was tested at different operating points modifying the drain voltage to assess its performance. In these preliminary tests, the drain voltage was changed from 28V to 16V with 4V step. Figure 37 and Figure 38 present the measured power gain and the PAE results from the evaluation board of the power amplifier (AFT20S015) at different operating points.

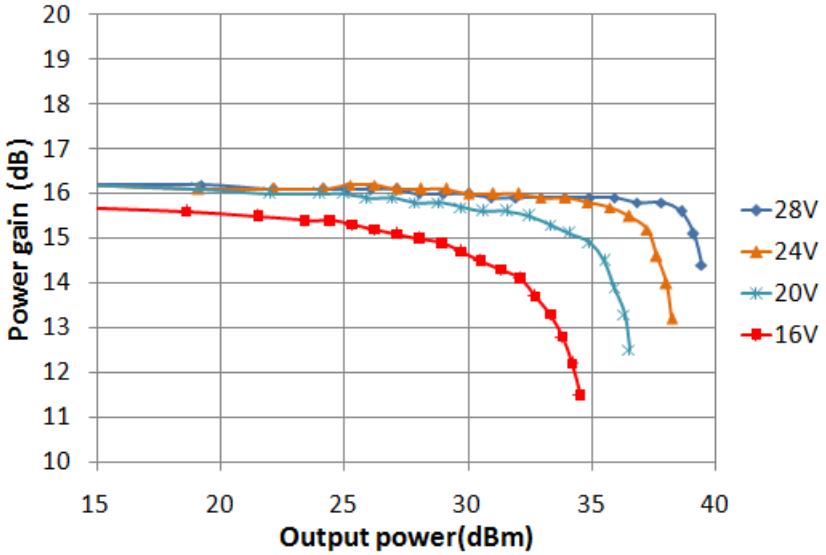



**Figure 37 Measured power gain from the evaluation board of the HPA – AFT20S015- at different operating points**

For 28V drain voltage, the 1dB compression output power is around 38 dBm as shown in Figure 37. For 24V drain voltage, it is approximately 37 dBm; for 20V drain voltage, it is about 34 dBm and for 16V drain voltage, it reduces up to 32 dBm. Depending on the CA configuration, different OBO levels are required at PA. Then the proposed solution will evaluate the best operating point to fulfil 3GPP specifications and improve energy efficiency. Figure 38 shows the PAE results demonstrating that the energy efficiency could improve using different operating points which should be optimized based on the PA requirements. This is the main objective of this evaluation and it is still under evaluation.

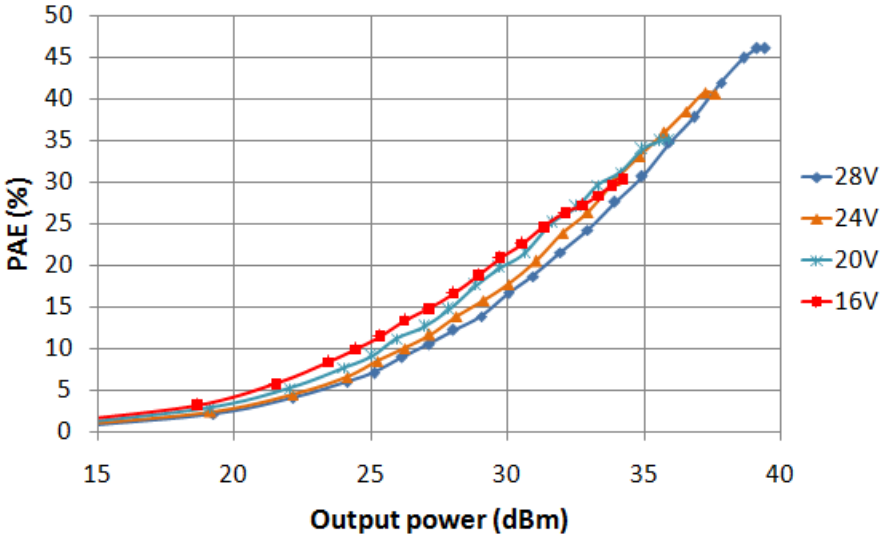



**Figure 38 Measured PAE results from the evaluation board of the HPA – AFT20S015– at different operating points**

Some preliminary tests have been done with E-TM1.1 signal for 1 CC, 2 CCs and 3 CCs in intra-band contiguous CA configuration (Figure 39, Figure 40, Figure 41). The measurements were done using a 30dB attenuator at the PA output, so the output power levels presented in figures should be increased by 31 dB due to the 30dB attenuator and the cable which were introduced during tests.

For 1 CC, the average output power to achieve ACLR results higher than 45dB is 23.8 dBm (-7.2dBm + 31dB) (Figure 39.This test was done with 28V drain voltage, then the drain voltage could be reduced to provide 15 dBm average output power and 45 dB ACLR results improving energy efficiency.

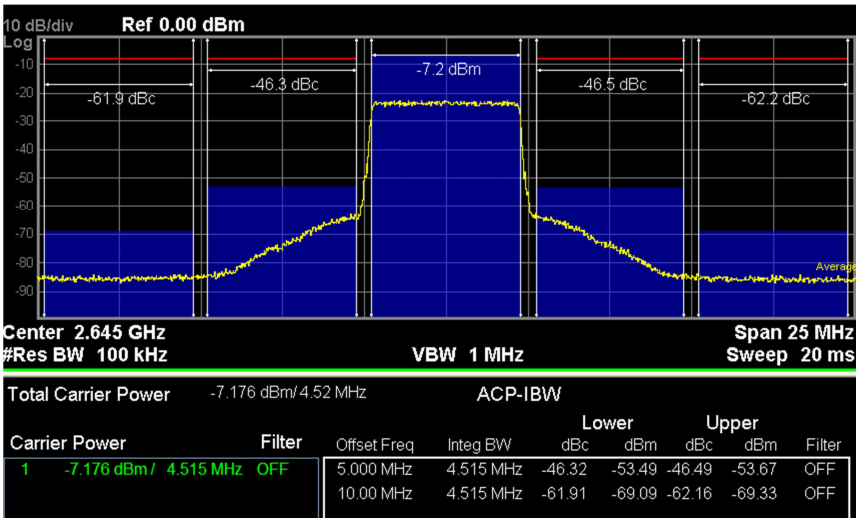



**Figure 39 ACLR test for 1CC at LTE band 7**

Figure 40 shows the ACLR test for 2 contiguous CCs at LTE band 7. In this configuration, the average output power to fulfil ACLR specification is around 20 dBm (considering 2CCs with 17dBm each). Two CCs with 15 dBm require 18 dBm average output power, again a different operating point could be defined to improve PAE.

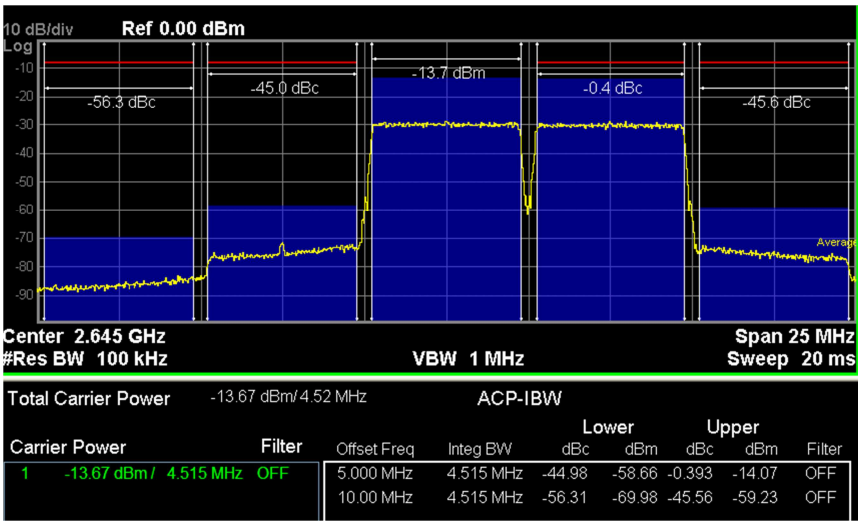



**Figure 40 ACLR test for 2 contiguous CCs at LTE band 7**

Finally for 3 contiguous CCs, the average output power to fulfil ACLR specification is around 18 dBm (considering 3CCs with 13.3dBm each) as shown Figure 41. In this case, the average output power per CC should be lower than 15 dBm, about 13.5 dBm.

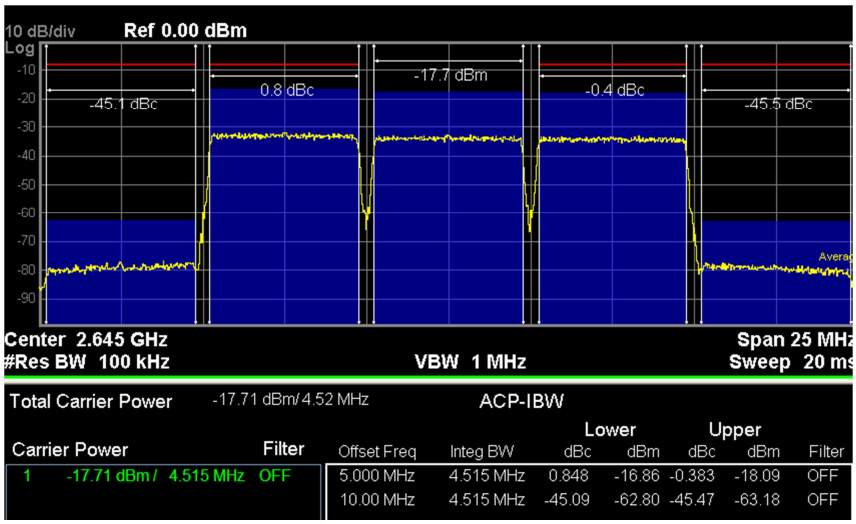



**Figure 41 ACLR test for 3 contiguous CCs at LTE band 7**

All these results are preliminary from the combination of the evaluation boards. In the final demonstrator, lower insertion losses are expected due to a higher integration level.

#### 2.3.1.2.7 Next steps

The different evaluation boards manufactured should be integrated for the final demonstrator. Furthermore, the power amplifier for LTE band 20 should be selected and tested.With the final hardware demonstrator, different tests will be carried out to evaluate the PA performance for different CA configurations and different operating points will be defined to fulfill 3GPP specifications and improve energy efficiency. Up to now, only preliminary tests were performed to define how tests will be done. E-TM test model signals were selected and specifically E-TM1.1 signal.

Moreover, these preliminary tests were only for intra-band contiguous CA. For the final validation, intra-band non-contiguous CA and inter-band CA will be also evaluated.

### 2.3.2 Multi-band frequency agile antenna system for carrier aggregation: implementation and experimental characterizations

#### *2.3.2.1 Selection of technology*

The selected antenna system is composed of a regular microstrip patch antenna for LTE band 7 and a more complex dual band frequency agile folded microstrip patch antenna for LTE band 20.

The strategy behind this design was to minimize the antenna system bandwidth as much as possible in order to minimize its size taking into account the different CA modes. Due to its lower operating frequency range, only band 20 antenna has required miniaturization in this antenna system.

The dimensions of band 20antenna have been reduced as much as possible until the bandwidth was reduced to two times 10MHz, which corresponds to the required instantaneous bandwidth for one pair of Rx and TX band 20 channels. Those two 10 MHz wide narrow sub-channels are 40MHz apart from each other. Frequency agility has then been introduced to make the antenna capable to cover band 20 entirely by switching from one channel to another. Two Digitally Tunable Capacitors (DTC) are used as frequency agility active components in this design. DTC have been selected because they have superior linearity performance compared to other tuning components such as varactor diodes.

At the end, the proposed antenna topology remains compatible with all the CA modes available at the RF front end while only taking up a volume of 66 x 54.5 x 23mm$^3$ ($\lambda_0$/5,7 x $\lambda_0$/7 x $\lambda_0$/16,5 with $\lambda_0$ = 379mm@791MHz).

The antenna topology selected is presented in details in deliverable [2].

#### *2.3.2.2 Platform implementation*

Based on the antenna design presented in [2], a prototype will be built and tested. As shown in Figure 42, the prototype will be made of a specifically designed PCB and both LTE band 7 and 20 antennas.

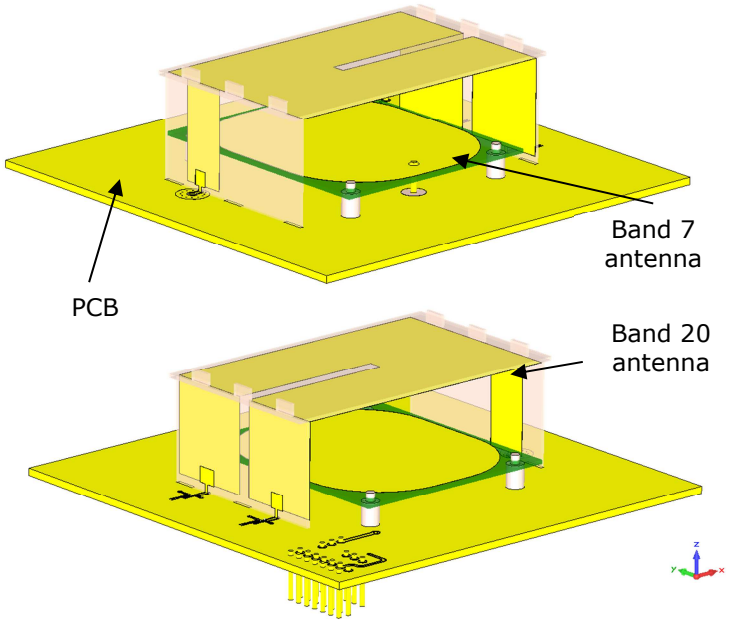



**Figure 42 3D views of the assembled prototype**

The PCB (Figure 43), which will act as reference ground plane for the antennas, will embed the electronic circuitry needed to control the frequency agile antenna system. The two Peregrine DTCs, which are used to make the antenna agile, will be controlled thanks to the same serial bus (Figure 44) as proposed in the datasheet. The control signals will be provided by the TTI RF front end board.

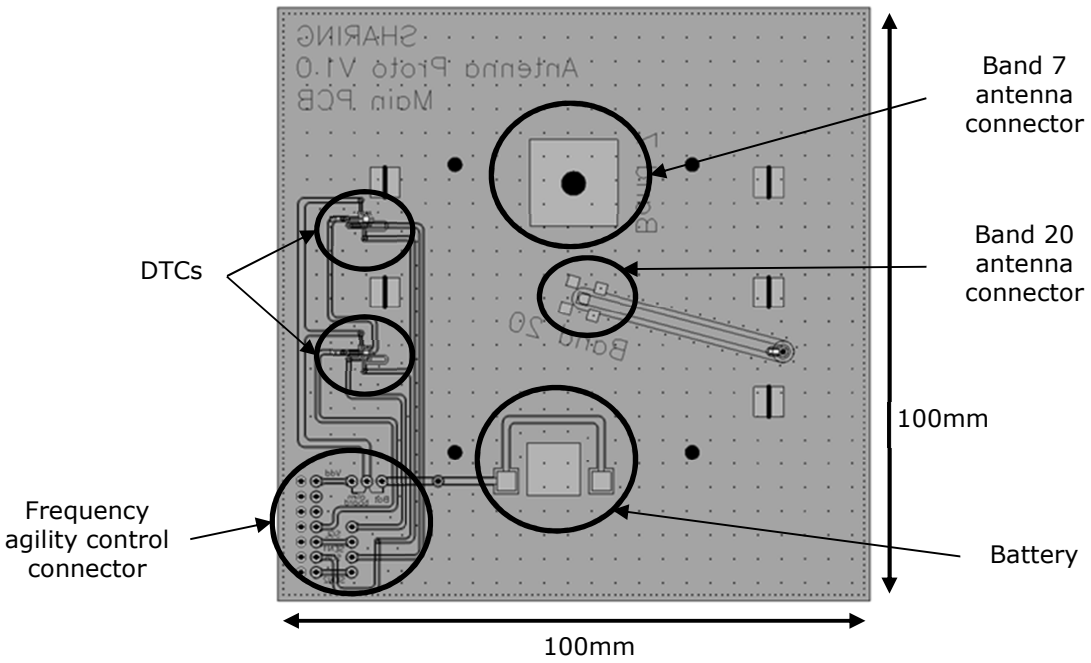



**Figure 43 Layout of the PCB designed for the antenna system**

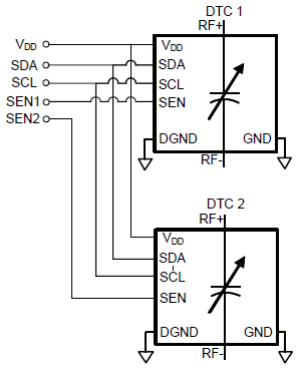



**Figure 44 DTC SPI bus sharing configuration**

Band 7 antenna will be printed on a 1mm thick FR4 (εr = 4.4 ; tanδ = 0.02) metallized substrate. It will be positioned 5 mm above the ground plane thanks to 4 nylon struts. Also, a SMA connector will be used as the feed line. The outer part of the SMA connector will be connected to the ground.

Band 20 antenna will be printed on three distinct low loss 0.813mm thick substrates (Rogers RO4003®: εr = 3.55; tanδ = 0.0027). They will be soldered together to form the antenna and then placed above the PCB and soldered to it.

As explained in [2] the fact that band 20 antenna lies just above band 7 antenna does not shadow the radiation coming from band 7 antenna because of their respective radiation mechanisms.

#### *2.3.2.3 Cable impact on antenna measurement*

Small antenna measurements must be carefully carried out in order to reach accurate results. In fact, the cable used for the measurement can easily disturb the antenna under measurement and thus lead to inaccurate measurement results. In our case, we have carried out a study of the measurement cable location in order to minimize its impact on the antennas.

It is better to place the cable orthogonally to the main polarization. In our case, both band 7 and band 20 antennas have their polarization parallel to the ground plane. This is why we have placed the measurement cable normally to the ground plane (along Z direction). Moreover, the main radiation of both antenna is oriented towards the upper hemisphere, thus, the measurement cable is placed on the back side of the ground plane as shown in Figure 45. Finally, in order to determine accurately the best

location for the measurement cable contact with the ground plane, a specific study has been carried out for both antenna measurement cables.

In the case of band 20 antenna, the size of the PCB is about λ/4 @791MHz (λ=379mm) , which is too small to avoid back radiation and surface current on the back side of the ground plane. As a result, the measurement cable is expected to disturb the measurement if not well placed.

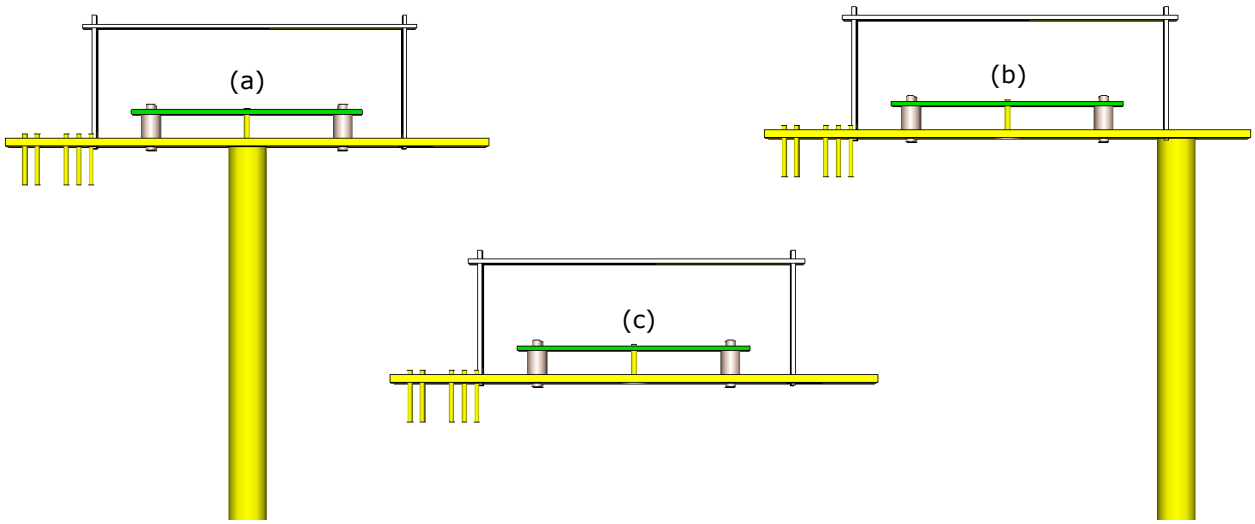



**Figure 45 Views of the prototype: (a) with the measurement cable placed in the middle of the PCB; (b) with the measurement cable placed on the side of the PCB; (c) without measurement cable.**

Figure 46 shows the simulated reflection coefficient of the band 20 antenna with the measurement cable placed in 2 distinct locations and without the measurement cable as described in Figure 45. When the cable is placed on the side of the ground plane (where band 20 feed point lies), the reflection coefficient (i.e. the impedance) is much more disturbed than when the cable is placed in the middle of the ground plane compared to the reflection coefficient obtained without the measurement cable. This means that the impact of the measurement cable is minimized when placed in the middle of the PCB.

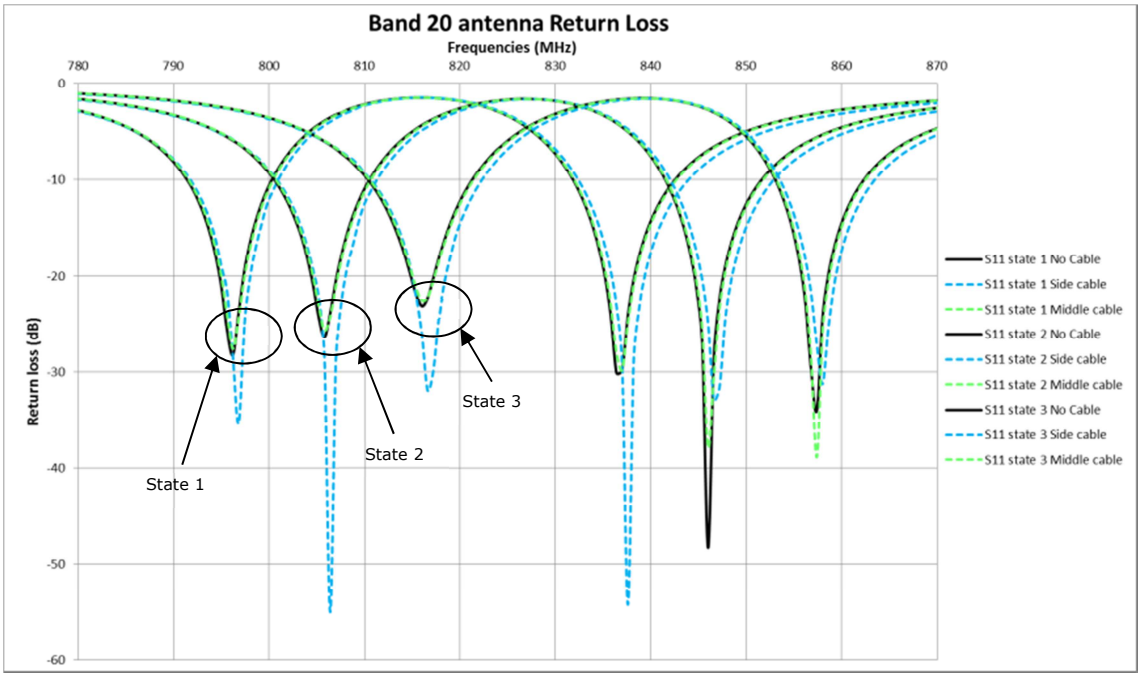



**Figure 46 Band 20 antenna reflection coefficient (black : without measurement cable ; dashed Blue : with a measurement cable on the side of the PCB ; dashed green : with the measurement cable on the middle of PCB)**

Figure 47 compares the realized gain pattern of band 20 antenna with the measurement cable placed in the middle of the PCB and without measurement cable. There is almost no difference between both configurations which means no perturbation due to the cable. This confirms that, in order to minimize the measurement cable impact on the measurements, it must be placed in the middle of the PCB.

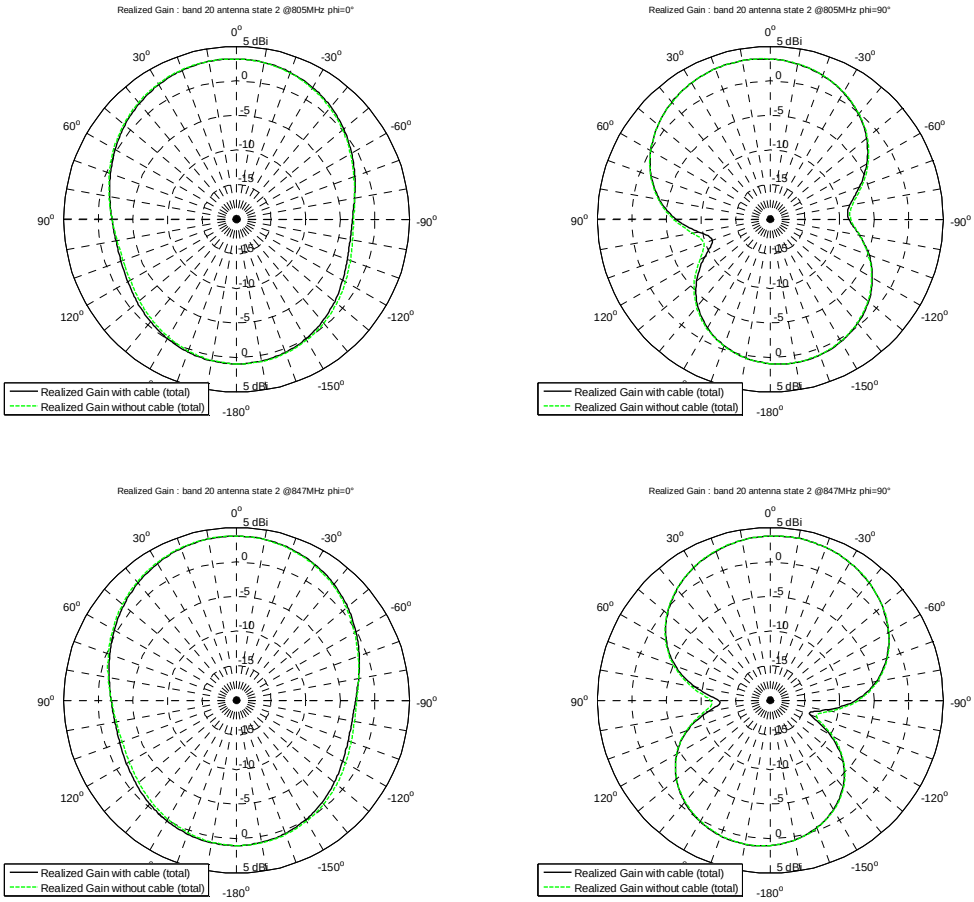



**Figure 47 Band 20 antenna realized gain pattern**

In the case of band 7 antenna, the width of the PCB (100mm) is almost one wavelength @2.5GHz (λ=120cm) and the antenna is not considered as a small antenna. Therefore, the measurement of this antenna should not be as problematic as for the band 20 antenna. However, it has been verified that the selected location of the measurement cable would not impact the antenna measurement.

Figure 48 and Figure 49 show almost no difference between respectively the impedance and the realized gain pattern simulation with and without the measurement cable. The cable can then be connected directly to the band 7 antenna access without disturbing the antenna measurement.

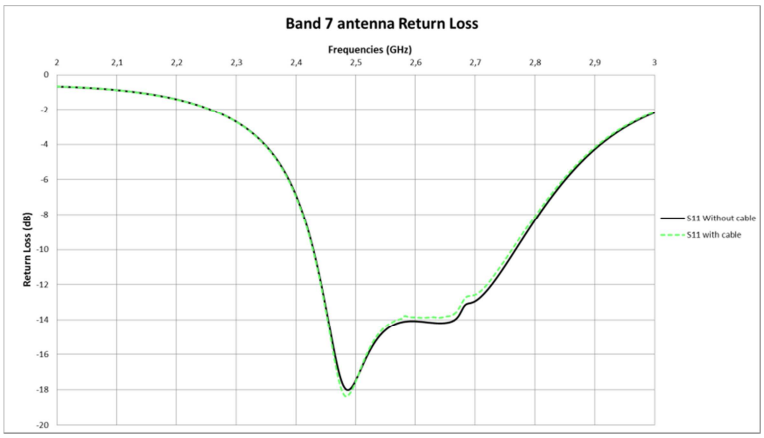



**Figure 48 Band 7 antenna reflection coefficient**

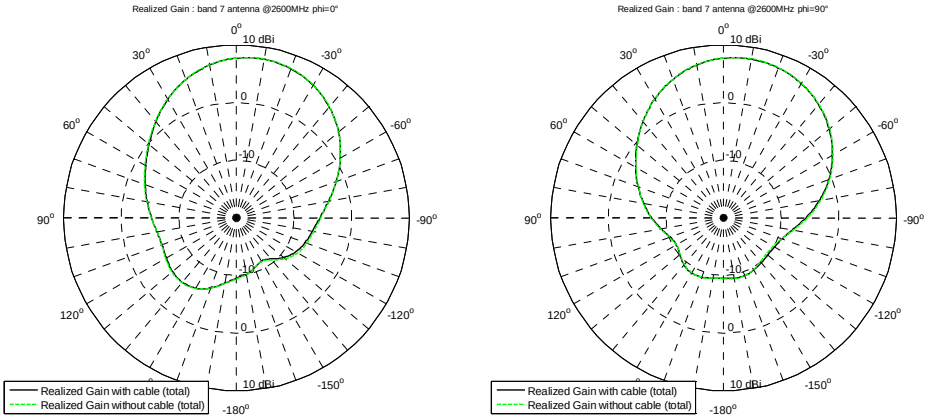



**Figure 49 Band 7 antenna realized gain pattern**

#### *2.3.2.4 Next steps*

A prototype is being built and will be measured. The impedance and radiation measurements campaign will validate the different techniques used in this design such as the frequency agility and the smart placement of both antennas that minimize their mutual coupling.

The gain level and radiation pattern will also be validated thanks the measurement campaign.

Once this antenna measurement campaign will be carried out, the TTI RF front end and the CEA antenna system will be connected and showcased together.

## 2.4 Use-case 4: Cellular Offloading

### 2.4.1 Mobile Data Offloading in Heterogeneous Wireless Networks based on Multiple Attribute Decision Making

Offloading cellular data to Wi-Fi is a promising candidate to overcome the capacity bottleneck of next generation cellular communication systems. However, selecting the best connection in a heterogeneous network is still an open research topic. Developing a centralized platform utilizing a multiple attribute decision making algorithm for heterogeneous wireless networks comes forward as a new solution for the optimal cellular to Wi-Fi offloading problem.

#### *2.4.1.1 Selection of Algorithm*

For Wi-Fi Offloading PoC that will be developed in this WP, mobile data offloading based on a Multiple Attribute Decision Making (MADM) algorithm: Technique for Order Preference by Similarity to Ideal Solution (TOPSIS) algorithm, is selected. In Section 4 of [4], the details of the TOPSIS algorithm are presented and evaluated.

TOPSIS algorithm [5], is selected due to its ease of implementation and adaptability to needs of different operators. Hence it forms a suitable basis to select the optimal target network for a given a set of given observed attributes for a user.

In the first step of TOPSIS algorithm a decision matrix **A** is created:

$$\mathbf{A} = \left[ a_{ij} \right] = \begin{bmatrix} a_{11} & a_{12} & \dots & a_{1m} \\ a_{21} & a_{22} & \dots & a_{2m} \\ . & . & \dots & . \\ . & . & \dots & . \\ . & . & \dots & . \\ a_{p1} & a_{p2} & \dots & a_{pm} \end{bmatrix} (i = 1, \dots, p;\ j = 1, \dots, m) \tag{2.12}$$

In matrix **A**, m refers to size of the multiple attribute set such as link quality, Mean Opinion Score (MOS) of the target network for the given application, user preference (cost security), etc and *p* refers to size of the multiple decision point set of networks which can be LTE, WLAN or D2D (device-to-device). Note that all the attributes are transformed to have positive impact if necessary.

In second step, a normalized decision matrix is formed by using the following equation:

$$r_{ij} = \frac{a_{ij}}{\sqrt{\sum_{k=1}^{p} a_{kj}^2}} \tag{2.13}$$

Then the normalized matrix R is obtained as:

$$\mathbf{R} = [r_{ij}] = \begin{bmatrix} r_{11} & r_{12} & \dots & r_{1m} \\ r_{21} & r_{22} & \dots & r_{2m} \\ . & & & . \\ . & & & . \\ . & & & . \\ r_{p1} & r_{p2} & \dots & r_{pm} \end{bmatrix} \tag{2.14}$$

In third step, a weighted normalized decision matrix is created by multiplying each column of the matrix by corresponding weight $w_i$ where $\sum_{i=1}^{m} w_i = 1$ by using the following equation:

$$\mathbf{v_i} = w_i * \mathbf{r_i}, \qquad \mathbf{r_i} = [r_{1i}, ...., r_{pi}]^T, \qquad i = \{1, 2, ..., m\} \tag{2.15}$$

In fourth step, the positive ( $A^*$ ) and negative ( $A^-$ )sets are formed by using the following formulas:

$$A^* = \left\{ (\max_i v_{ij} \,|\, i \in \{1, 2, ..p\}) \right\} \tag{2.16}$$

$$A^- = \left\{ (\min_i v_{ij} \,|\, i \in \{1, 2, ...p\}) \right\},\ j = \{1, ..., m\}$$

At the end of fourth step, sets are formed as $A^* = \{v_1^*, v_2^*, ..., v_m^*\}$ and $A^- = \{v_1^-, v_2^-, ..., v_m^-\}$.

By calculating the Euclidean distance $S_i^*$ of each multiple decision point from the positive point $A^*$ and $S_i^-$ of eachmultiple decision point from the negative point $A^-$ .

$$S_i^* = \sqrt{\sum_{j=1}^{m} (v_{ij} - v_j^*)^2}, \quad i = \{1, ..., p\} \tag{2.17}$$

$$S_i^- = \sqrt{\sum_{j=1}^{m} (v_{ij} - v_j^-)^2}, \quad i = \{1, ..., p\}$$

In the final step, the relative similarity of the alternatives from the positive and negative points is calculated as:

$$C_i = \frac{S_i^-}{S_i^- + S_i^*}, \quad i = \{1, ..., p\} \tag{2.18}$$

where $0 \le C_i \le 1$.

The final solution is selected by:

$$e^* = e_{i^*} \qquad \text{where } i^* = \arg\max_i C_i, \quad i = \{1, ..., p\} \tag{2.19}$$

#### *2.4.1.2 Platform Implementation*

In the SHARING project, a PoC platform for heterogeneous wireless networks is developed to present a centrally controlled Wi-Fi Offloading mechanism. To enable this mechanism, several attributes, such as user's connection statistics and terminal status, are periodically collected from terminals via an installed mobile application and sent to a remote server called SHARING Server. The server runs the MADM algorithm, TOPSIS, and the decision on the best network connection is sent back to terminals for execution.

##### 2.4.1.2.1 Requirements

- Server
  - Processor: min 2.0GHz
  - RAM: min 1GB
  - HDD: min 250MB
  - Software: Linux, Apache Tomcat
- Mobile Phone
  - Android v4.3.1
  - EAP-SIM support
- Wi-Fi Access Point
  - 802.11a, 802.11b, 802.11g or 802.11n
  - EAP-SIM support
- 3G Cellular Internet Access
  - Bit Rate: min HSPA

#### 2.4.1.2.2 Architecture

The platform architecture is provided in Figure 50. The PoC platform will be implemented in two phases. In the first phase the SHARING Server will only be connected to the user terminal to receive attributes for decision making via REST API. In the second (final) phase the SHARING Server will be connected to mobile core network and Wi-Fi core network via infrastructure APIs to acquire system level attributes as well.

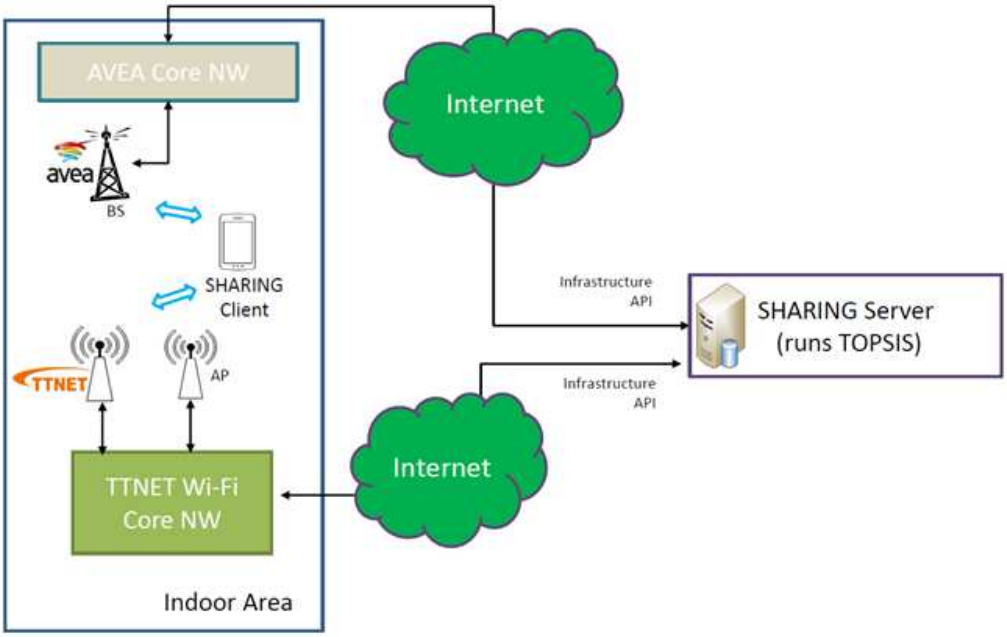



**Figure 50 High Level Wi-Fi Offloading Architecture**

#### 2.4.1.2.3 Software Design

In this part, the building blocks of the implementation are provided.

##### 2.4.1.2.3.1 Client

The software design of the SHARING Client application for WiFi offloading is provided in Figure 51

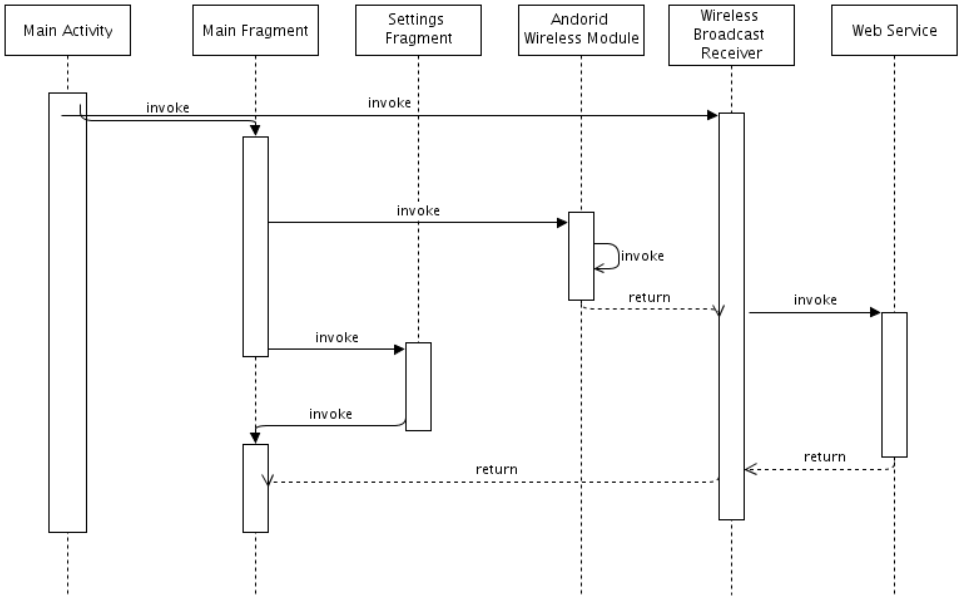



**Figure 51 SHARING Client Sequence Diagram**

The descriptions of the main modules of the application are provided below.

**Main Activity**: This is the main part of the SHARING client application. It triggers two parts of the application. The main fragments and wireless broadcast receiver.

**Main Fragment**: This is main User Interface screen of the application listing the access points (3G and WiFi) as shown in Figure 52.

**Settings Fragment**: This module includes the application's settings. It can also include the weights of features of the MADM algorithm.

**Android Wireless Module (AWM)**: This is the built-in wireless module installed in the device. This module scans the wireless access points (3G and WiFi) and sends access point lists and network state changes (shutdown of Wireless, connected to another WiFi, etc.) to wireless broadcast receiver with the return command. This module runs periodically or via panic button in main fragment for scanning. Current value of scanning period is 10 sec.

**Wireless Broadcast Receiver (WBR)**: This module processes the received information from Android Wireless Module. If information received from AWM is "scan result", then WBR sends all AP list to server side via web service. If response "return" from Web Service is received or the information received from AWM is "network state changed" then WBR sends this information to Main Fragment via "return".

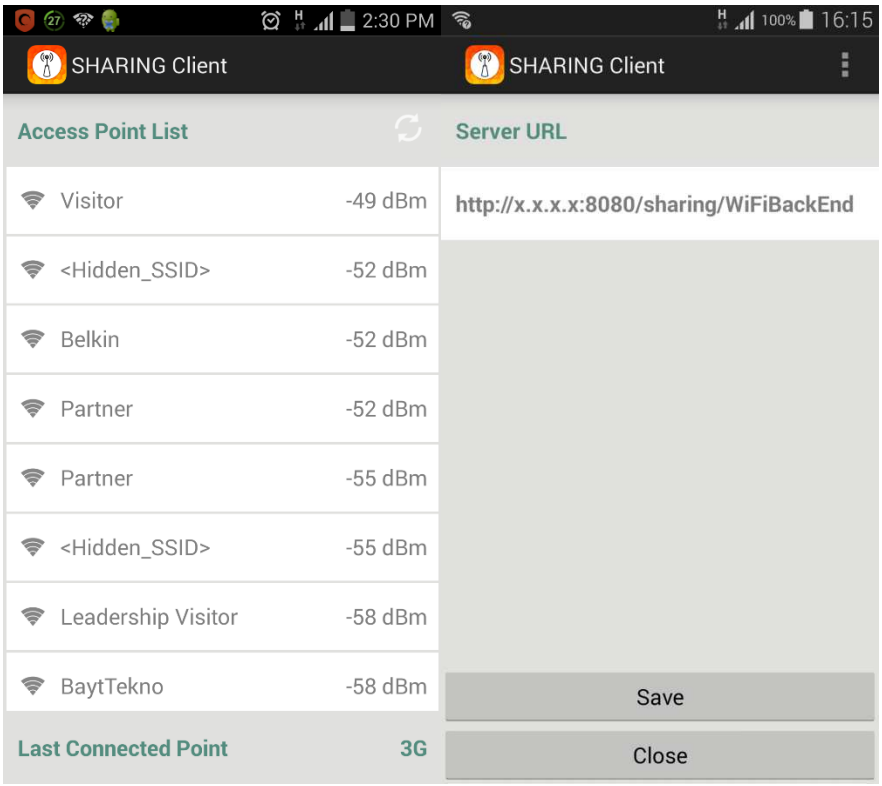



**Figure 52 SHARING Client Android Application User Interface**

#### 2.4.1.2.3.2 Server (Web Service)

The SHARING server runs the MADM algorithm called TOPSIS. Basically the server has three interfaces. One of the interfaces which is called Client API receives client related parameters, RSSI, battery level, roaming/non-roaming status, through HTTP communication from SHARING client. Client API is also used to send the network connection decision from SHARING server to SHARING client. The other interface is a REST-based web service interface called Infrastructure API. The Infrastructure API can obtain offline (statistical and long term measurements) or real-time data from operators. Based on operator agreements, the Infrastructure API can provide channel utilization ratio, latency, number of active Packet Data Protocol (PDP) connections, network congestion ratio as well as backhaul Internet connectivity status of WLAN and cellular network operators to SHARING server. The last web interface is REST-based Registration API. Through this API, third parties can register the access point credentials to SHARING server database. The information collected from all three APIs (such as SSID, BSSID,

capabilities, frequency and password as well as cellular network parameters of users) are stored in the database inside SHARING server.

#### 2.4.1.2.4 DemonstrationScenario

1. (Phase-1&2) The user installs the SHARING client application to their mobile terminal.
2. (Phase-1&2) The terminal enters a heterogeneous wireless network access area where there is at least one Wi-Fi AP and one 3G BS access.
3. (Phase-1&2) The SHARING client application sends network connection statistics and mobile phone status (e.g. battery level) to the SHARING Server.
4. (Phase-2) Wi-Fi core network and 3G Core network metrics are sent to the SHARING Server periodically.
5. (Phase-1&2) Based on the collected network and mobile terminal metrics, SHARING Server calculates the best network connection using the multiple attribute decision making algorithm and sends the decision to the SHARING client installed on the mobile terminal.
6. (Phase-1&2) Based on the decision sent by SHARING server, SHARING client selects the network for the mobile terminal.

### 2.4.2 Next steps

The technical work plan for the implementation and integration of mobile data offloading is provided in Section 2.4.1.2.4. In the first phase, which is planned to be completed by mid-2015, SHARING server and client will be developed and the attributes only based on mobile terminal will be collected. In the second phase, which is planned to be completed by end of 2015, integration interfaces with the core network will be developed to enable collection of network level attributes for system level optimal cellular offloading.

The development of mobile data offloading platform within the SHARING project is performed in parallel with another commercial Wi-Fi Offloading project within AVEA. The commercial AVEA Wi-Fi offloading project utilizes EAP-SIM authentication and as of early 2015 it is in the test phase. However, the project does not include optimal offloading decisions, i.e. mobile terminal switches to AVEA Wi-Fi access points where available. The outcomes of the mobile data offloading with MADM technique developed within the SHARING project is planned to be integrated to the commercial AVEA Wi-Fi Offloading system in 2016

## 2.5 Use Case 5 Reconfigurable and Low Power Filter Bank Implementation based on Dynamic Partial Reconfiguration in FPGAs

Dynamic partial reconfiguration is an advanced FPGA technique which improves the flexibility and reduces dynamic and static power consumption. The scope of this proof of concept is to implement a reconfigurable low power filter bank. The filter will use advanced techniques to adjust the bandwidth and cut off frequency using small number of parameters. Reconfigurable filter bank mechanisms with complete control over variable subband bandwidths have been proposed for future multiple-standard wireless communication receivers. Our scenario will be designed in the aim to prove experimentally that reconfigurable filter bank using FPGA dynamic partial reconfiguration can make the best trade off between energy saving, reconfiguration time and performance.

### 2.5.1 Selection of algorithm

In cognitive radio, the channelizer needs to be reconfigurable so as to transmit/receive channels of any arbitrary bandwidth and any center frequency corresponding to multiple communication standards. Operations such as channelization and spectrum sensing are usually performed using a filter bank (FB). The FB must be dynamically reconfigurable which means that the same filter bank can be reconfigured for a desired frequency specifications with minimum hardware complexity overhead, instead of employing separate filter banks for each specification. The digital filter bank is responsible for the channel selection task which involves inter-standard channel bandwidth variations (GSM: 200 kHz, 3G FDD: 5 MHz), as well as intra-standard channel bandwidth variations (LTE: 1.25 MHz-20 MHz). Consequently, the filter bank must have linear phase and should be dynamically reconfigurable, that is, it should have complete control over its frequency parameters (i.e., number of sub-bands, sub band's bandwidth, sub band's center frequency). A number of different digital filter bank design approach are available in literature [6]-[9]. The discrete Fourier transform filter bank (DFTFB) consists of prototype filter implemented in poly-phase form followed by Inverse Discrete Fourier Transform (IDFT). The DFTFB (Figure 53) has the drawbacks of uniform sub-band bandwidth and fixed center frequency for each sub-band.

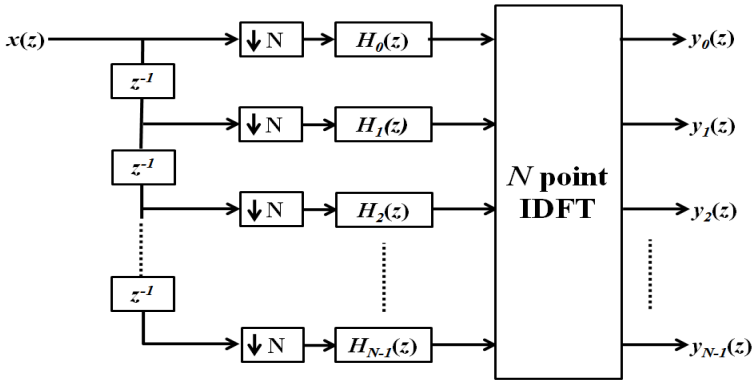



**Figure 53 Discrete Fourier transform filter bank**

An improved DFTFB architecture (Figure 54) using coefficient decimation method (CDM) has been used in [8]. By controlling CDM factor, $D_{II}$, passband width of the prototype filter and hence, sub-band bandwidth can be varied. However, it provides only coarse control over sub-band bandwidth because the decimation factor is restricted to be integer.

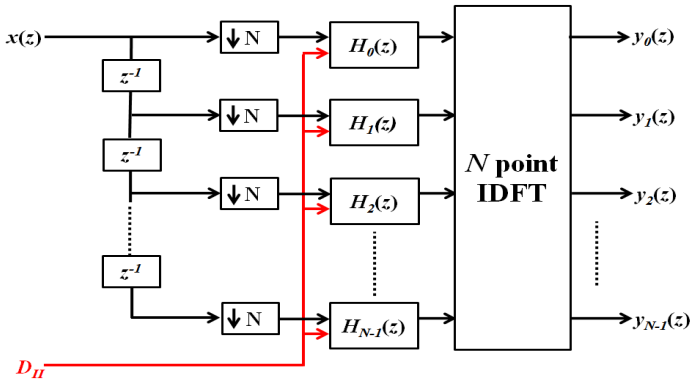



**Figure 54: CDM- Discrete Fourier transform filter bank**

Another efficient implementation of filter banks is the fast filter bank (FFB) proposed in [10]. It is a low-complexity alternative and is suitable for application requiring sharp transition bandwidth. The main drawback of the FFB is the inability to provide non-uniform bandwidth sub-bands and fixed center frequency for each sub-band. Further improvements of the FFB have been developed such as the multiresolution fast filter bank MRFB and the reconfigurable fast filter bank RFFB (Figure 55). The MRFB and the RFFD allow coarse and fine control over the sub-bands bandwidth but the center frequency of sub-bands is fixed. All filter banks mentioned above cannot provide an integral and independent control over the bandwidth and the center frequency of each sub-bands.

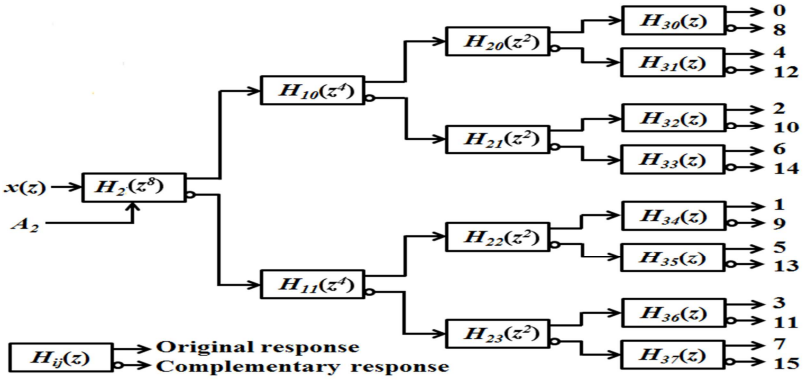



**Figure 55: Reconfigurable fast filter bank (RFFB)**

In this deliverable, we propose to implement in FPGA the linear-phase reconfigurable filter-bank called SPA-MCDM-FB [11], which is designed using the Spectral Parameter Approximation based Variable Digital Filters (SPA-VDFs) [12],[13], as well as exclusive Multiband response Capability of the modified coefficient Decimation Method (MCDM)[14],[15].The SPA-VDFs filters will be implemented using the Farrow structure. The SPA-MCDM-FB architecture allows an unabridged and independent control over the bandwidth and the center frequency of each sub-band over the entire Nyquist band without any hardware reimplementation or coefficient updates.

#### *2.5.1.1 SPA-MCDM Filter Bank*

The linear phase SPA-MCDM-FB is designed using the SPA-MCDM variable digital filter. It provides independent and individual control over the bandwidth and center frequencies of sub-bands. The SPA-based variable digital filter (Figure 56) was designed using the Farrow structure and has advantages of linear phase and very lower group delay. It provides a continuous control over entire range. However, the main drawbacks are as follows:

- The gate count complexity and group delay of SPA-VDF increases significantly with the increase in cut-off frequency range.
- The coefficient values of the sub-filters in SPA-VDFs increase exponentially with their order which may impose constraints when fixed-point implementation is needed.

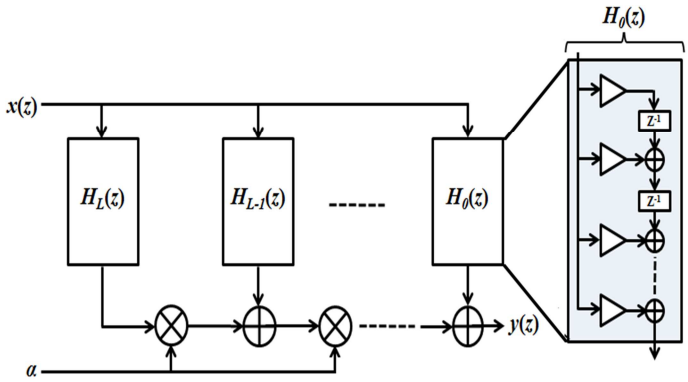



**Figure 56 Spectral Parameter Approximation based variable digital filter (SPA-VDF)**

In the modified-coefficient-decimation-method-based variable digital filter, a low-pass prototype filter is decimated by a factor *D*, *i.e.*, every $D^{th}$ coefficient is retained and the sign of every alternate retained coefficient is reversed. All other coefficients are replaced by zeros. This results in a multi-band frequency response with center frequency locations of the sub-bands given by odd multiples of $\pi/D$. In [11], authors design and propose an architecture for the *M* sub-band SPA-MCDM-FB as shown as in Figure 57.

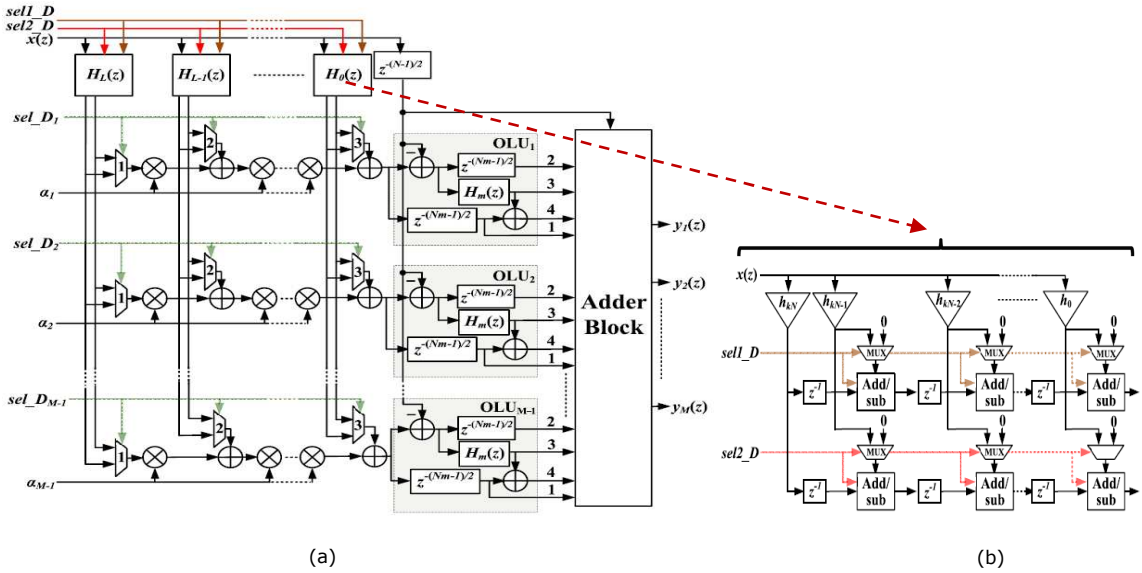



**Figure 57: (a) Architecture of the SPA-MCDM-FB [11], (b) Architecture of sub-filter**

### 2.5.2 Platform implementation

#### *2.5.2.1 Scenario: spectrum sensing*

Consider a case for dynamic spectrum sharing between different operators in systems with carrier aggregation (CA) which is an important feature in 3GPP LTE-A systems. We implement a simple scenario where the wideband input signal of 6 MHz bandwidth consists of multiple channels of bandwidths ranging from 200 kHz to 1.4 MHz. The locations and bandwidth of channel may vary dynamically. The digital front end (DFE) extracts the channel of interest and passed it to the demodulator block for further baseband processing. In addition, the DFE also selects the desired frequency band and passes it to the detector block to check whether the frequency band is vacant or not. Using conventional filter bank such as DFTFB, 32-subband filter bank is required since the resolution of filter bank is decided by the smallest channel bandwidth. For the scenario considered here, 5-subband SPA-MCDM filter bank which provides two band pass responses, one for channelization and other for spectrum sensing is used. The bandwidth and the center frequency of each band pass response can be controlled independently. To reduce power consumption, FPGA dynamic partial reconfiguration will be used and different measurements of static/dynamic power consumption will be given.

#### *2.5.2.2 Experimental setup*

The proposed architecture of the reconfigurable filter bank (SPA-MCDM-FB) will be implemented and evaluated on the Zynq-7000 AP SoC ZC702 with the Analog Devices AD-FMCOMMS3-EBZ FMC module featuring the AD9361 integrated RF Agile Transceiver.

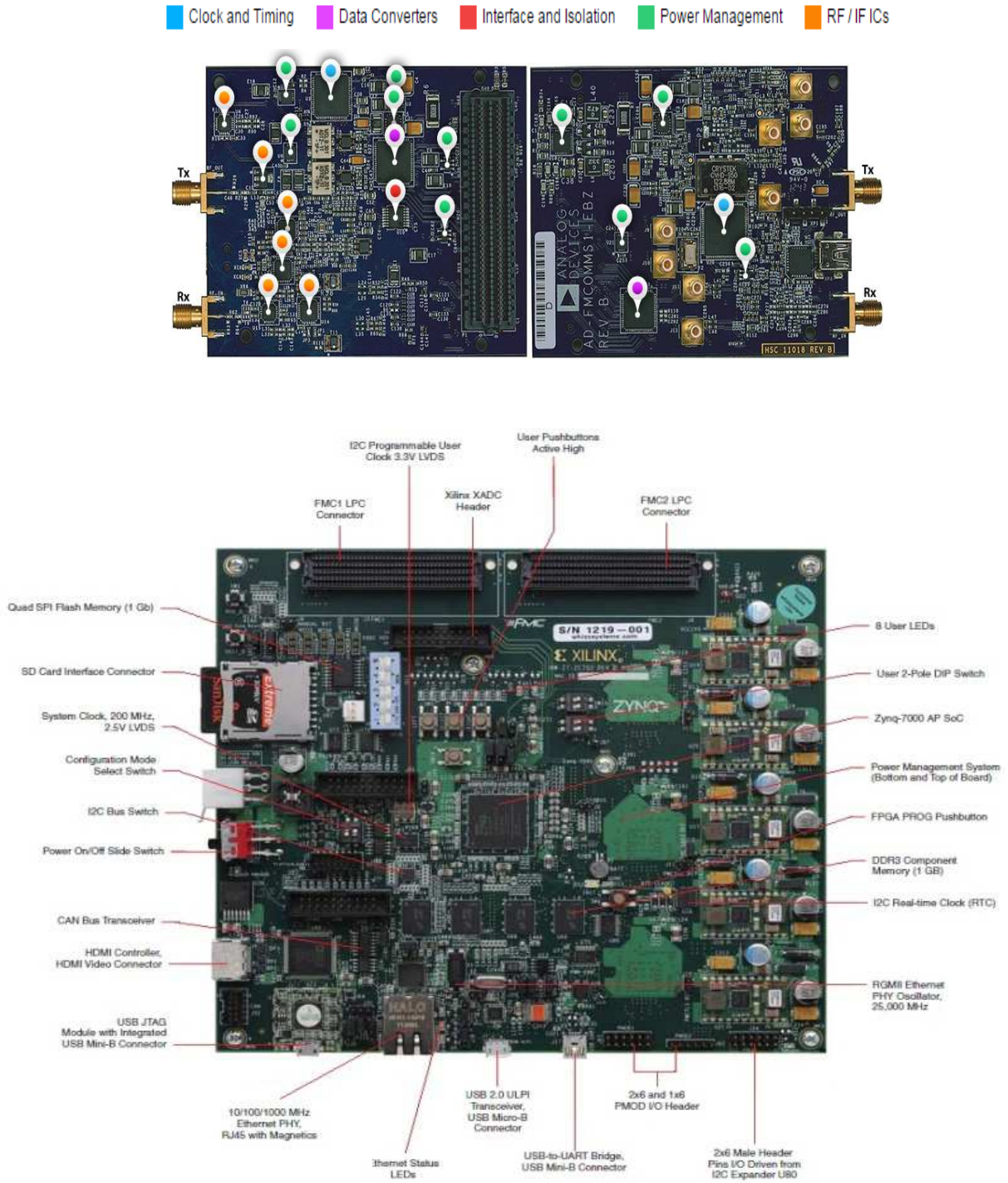



**Figure 58 (top) FMCOMMS1-EBZ mezzanine card[16], (bottom)Xilinx Zynq-7000 All Programmable SoC ZC 702 [17]**

The Zynq-7000 platform consists of two parts, namely the Programmable Logic (PL) and the Processing System (PS). The PL consists of an Artix-7 FPGA fabric with 85K logic cells. The PL allows dynamic partial reconfiguration, which means to reconfigure a certain region of logic while the rest of the hardware keeps processing. The PS includes a dual-core ARM Cortex-A9 processor running at 667MHz. The PS is linked to the PL through an AMBAAXI bus, and hence the FPGA fabric can accommodate hardware accelerator modules circuits that accelerate the computation performed by the ARM. The PS and the PL use independent power supplies, with 1.0 V supply for the logic, 1.8 – 3.3 V for the input/output buffer bank and 1.2 – 1.8 V for the external dynamic memory interface. The FMCOMMS1-EBZ provides the analog front-end operates over a wide RF tuning range from 400 MHz – 4 GHz with 125MHz channel bandwidth (250 MSPS ADC, 1GSPS DAC).

#### 2.5.2.3 Architecture of SPA-MCDM filter bank

Given the architecture of the reconfigurable SPA-MCDM-FB in Figure 57(a), we can notice that the structure of the filter bank contains a huge number of multiplexers which consume a relatively large area and power. This approach is called classical approach of reconfiguration. In this case, designer uses multiplexers to select one and only one filter bank configuration. Multiplexer-based approaches assume the reconfiguration delay is a constant number(*i.e.* one clock rising edge).In order to meet all the objectives (Low-power consumption, reconfigurability, low reconfiguration overhead), the FPGA dynamic partial reconfiguration (DPR) technique can be used since the various filters have many similarities in their structure. Therefore, dynamic partial reconfiguration addresses low power, coefficient flexibility and low reconfiguration time.

Xilinx suggests two basic styles of dynamic reconfiguration on a FPGA: the module-based partial reconfiguration and the difference-based partial reconfiguration. The former approach is closely related to modular design concepts to reconfigure large blocks of logic. The distinct blocks of the design to be reconfigured are known as reconfigurable modules. The latter approach can be used when a small change is made to the design. The generated partial bit stream contains only information about differences between the current design structure and the new design structure. Therefore, switching from one configuration to another can be done very quickly. Using the difference-based partial reconfiguration, the configuration of individual FPGA logic elements (*i.e.* LUT, memory content) are modified, but no module-level changes are performed. An example of this mode might be the dynamic modification of generator polynomials of convolutional encoder.

The basic SPA-MCDM-FB and sub-filters hardware architectures, shown in Figure 57 (a) and Figure 57 (b), have a huge number of multiplexers commanded by *M-1* signals, $sel\_D_i$ where *i=1..M-1*, and two signals {*sel1_D*, *sel2_D*} respectively. In this deliverable, we present an approach for implementing reconfigurable SPA-MCDM filter bank that uses FPGA dynamic partial reconfiguration.

In dynamic partial reconfiguration (DPR), the FPGA is divided in partial reconfiguration regions (PRR) with limited reconfiguration area, associated with a static region (SR) and bus macros (BMs) that are used to communicate the SR with the PRRs. Moreover, the DPR allows some of the logic on a FPGA (*i.e. PRRs*) to be reconfigured while the rest continues to operate. Figure 59 represents the overall architecture of the implemented reconfigurable filter bank. The design is composed of (*M-1*) output logic units (OLU), each of them consists of a fixed-coefficient masking filter,and (L+1) sub-filters, whose detailed architecture is depicted in Figure 60.

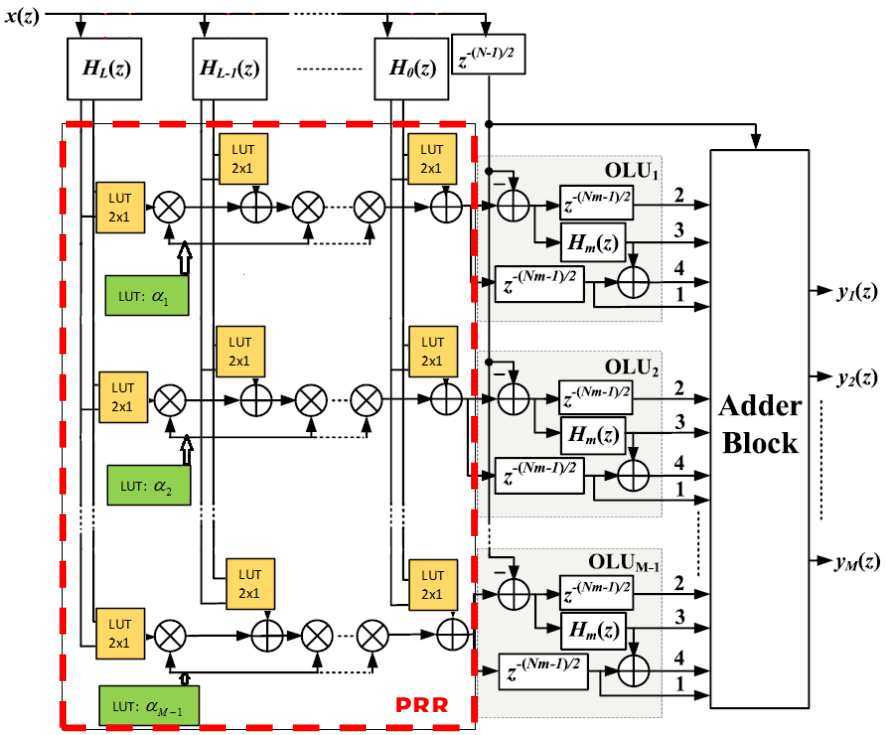



**Figure 59: Proposed SPA-MCDM Filter bank architecture using DPR approach**

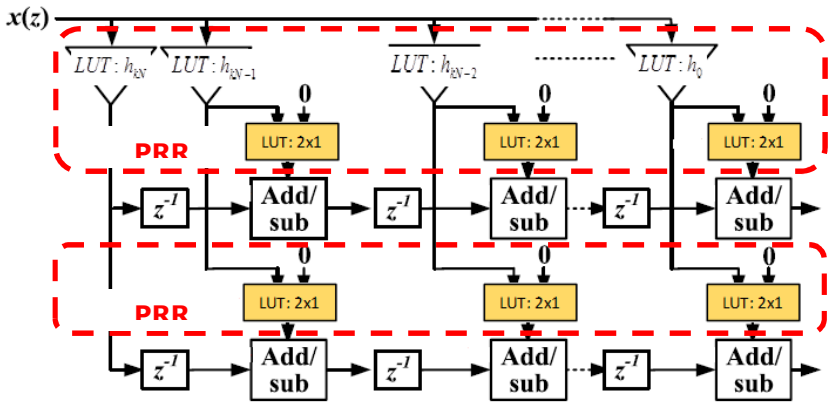



**Figure 60 Proposed sub-filters architecture using DPR approach**

#### *2.5.2.4 Next step*

Our Scenario was developed using universal software radio peripheral (USRP) N210 board with WBX 50-2200 MHz daughterboard and Gun Radio. The SPA-MCDM-FB will be implemented on Xilinx ZC702 hardware platform using FPGA dynamic partial reconfiguration and evaluated using a real environment (Scenario1). We will compare the reconfiguration time between our design approach and the classical implementation approach. Moreover, the static and the dynamic power will be evaluated using ZC702 board. We plan to finish the implementation and evaluation aspects on September 2015.

# 3 Conclusion

In this document, the key algorithms and technologies that will be integrated in the various demonstrators were described in detail, as well as the building blocks of the corresponding PoCs, namely:

- Relaying in two different contexts: eMBMS relays for coverage extension of eMBMS multicast-broadcast services and Device-to-device (D2D) communications for content delivery reusing uplink resources.
- Cooperative Multipoint (CoMP) transmission coupled with interference rejection in User Equipment (UE) and Multiuser-MIMO (MU-MIMO)
- Advanced RF architectures in support of Carrier Aggregation (CA)
- WIFI Offloading
- FPGA reconfigurability for low-power filter banks implementation

The next deliverable D7.3 will describe the results of the integration and some initial test results, while the final deliverable D7.4 will contain the final proof of concept validation, results and analysis.

# 4 List of Abbreviations, Acronyms, and Definitions

| | |
|---|---|
| 3GPP | Third Generation Partnership Project |
| ACK/NAK | Acknowledgement/Negative acknowledgement |
| ACLR | Adjacent Carrier Leakage Ratio |
| API | Application Programming Interface |
| BM | Bus Macro |
| BS | Base Station |
| CA | Carrier Aggregation |
| CBA | Contention-Based Access |
| CC | Component Carrier |
| CCDF | Complementary Cumulative Distribution Function |
| COTS | Commercial Off-The-Shelf |
| CRC | Cyclic Redundancy Check |
| DC | Direct Current |
| DCI | Downlink Control Information |
| D2D | Device-to-Device |
| DFTFB | Discrete Fourier transform filter bank |
| DMRS | Demodulation reference signal |
| DPR | Dynamic Partial Reconfiguration |
| DTC | Digitally Tunable Capacitors |
| EPC | Evolved Packet Core |
| E-TM | E-UTRA Test Model |
| E-UTRA | Evolved Universal Terrestrial Radio Access |
| FB | Filter Bank |
| FDD | Frequency Division Duplex |
| FFB | Fast Filter Bank |
| FFS | For Future Study |
| FFT | Fast Fourier Transform |
| FPGA | Field Programmable Gate Array |
| HARQ | Hybrid Automatic Repeat Request |
| HPA | High Power Amplifier |
| IA-ML | Interference Aware Maximum Likelihood |
| IDFT | Inverse Discrete Fourier Transform |
| LDMOS | Laterally Diffused Metal Oxide Semiconductor |
| LLR | Log Likelihood Ratio |
| LSB | Less Significant Bit |
| LTE | Long Term Evolution |

| | |
|---|---|
| LTE-A | Long Term Evolution - Advanced |
| MAC | Medium Access Control |
| MADM | Multiple Attribute Decision Making |
| MBMS | Multimedia Broadcast/Multicast Service |
| MBSFN | Multicast Broadcast Single Frequency Network |
| MCS | Modulation and Coding Scheme |
| MOS | Mean Opinion Score |
| MRFFB | Multi-resolution Fast Filter Bank |
| NAS | Non Access Stratum |
| OAI | Open Air Interface |
| OBO | Output Back Off |
| OIP3 | Third Output Intermodulation Power |
| PA | Power Amplifier |
| PAE | Power Added Efficiency |
| PAPR | Peak to Average Power Ratio |
| PCB | Printed Circuit Board |
| PDCP | Packet Data Convergence Protocol |
| PDP | Packet Data Protocol |
| PHY | Physical Layer |
| PLMN | Public Land Mobile Network |
| PoC | Proof of Concept |
| PRB | Physical Resource Block |
| PRR | Partial Reconfiguration Region |
| PUCCH | Physical Uplink Control Channel |
| PUSCH | Physical Uplink Shared Channel |
| REST | REpresentational State Transfer |
| RFFB | Reconfigurable Fast Filter Bank |
| RLC | Radio Link Control |
| RA-RNTI | Random Access Radio Network Temporary Identifier |
| RRC | Radio Resource Control |
| SL-MMSE | Single Layer-Minimum Mean Square Error |
| SMA | SubMiniature version A |
| SPA | Spectral Parameter Approximation |
| TCXO | Temperature Compensated Crystal Oscillator |
| TDD | Time Division Duplex |
| TX | Transmitter |
| UE | User Equipment |
| VCO | Voltage Controlled Oscillator |
| VDF | Variable Digital Filter |

# 5 Annex A

The computation of LLRs for a QPSK modulation with Gray code is presented here.

The equalized constellation point is given by:

$$\hat{x}_0 = \boldsymbol{b}\,\boldsymbol{g_e}\,x + \sum_{i=1}^{2} \boldsymbol{b}\,\boldsymbol{g_i}\,x_i + \boldsymbol{b}\,\boldsymbol{z}$$

with $\hat{x}_0 = \boldsymbol{b}^H \boldsymbol{y}$.

It must be noted that $\boldsymbol{b}\,\boldsymbol{g_e}$ is a real scalar. Indeed, remenbering that the MMSE filter can be written $\boldsymbol{b} = \boldsymbol{R}^{-1}\boldsymbol{g_e}$, with $\boldsymbol{R}$ an hermitian matrix:

$\boldsymbol{b}\,\boldsymbol{g_e} = (\boldsymbol{R}^{-1}\boldsymbol{g_e})^H \boldsymbol{g_e}$

And $\boldsymbol{b}\,\boldsymbol{g_e} = \boldsymbol{g_e}^H (R^{-1})^H \boldsymbol{g_e} = \boldsymbol{g_e}^H (R^H)^{-1} \boldsymbol{g_e} = \boldsymbol{g_e}^H R^{-1} \boldsymbol{g_e} = \boldsymbol{g_e}^H \boldsymbol{b}^H = (\boldsymbol{b}\boldsymbol{g_e})^H$

However, $\boldsymbol{b}\,\boldsymbol{g_i}$ is complex.

The first and second order moments of $\hat{x}_0$ are respectively:

$E[\hat{x}_0] = \boldsymbol{b}\,\boldsymbol{g_e} x_0 + \sum_{i=1}^{2} \boldsymbol{b}\,\boldsymbol{g_i}\,x_i$, and $\sigma^2 = E[|\hat{x}_0 - E[\hat{x}_0]|^2] = \boldsymbol{b}\boldsymbol{b}^H N_0$.

Therefore $E[\hat{x}_{0,I}] = \boldsymbol{b}\boldsymbol{g_e} x_{0,I} + Re\{\sum_i \boldsymbol{b}\boldsymbol{g_i} x_i\}$ et $E[\hat{x}_{0,Q}] = \boldsymbol{b}\boldsymbol{g_e} x_{0,Q} + Im\{\sum_i \boldsymbol{b}\boldsymbol{g_i} x_i\}$.

For the QPSK constellation, let's define the following notations:

$\alpha = \frac{\sqrt{2}}{2}\boldsymbol{b}\,\boldsymbol{g_e}$, $\alpha$ real

$\varphi = \sum_{i=1}^{2} \boldsymbol{b}\,\boldsymbol{g_i}\,x_i = \varphi_I + j\varphi_Q$, $\varphi$ complex.

The LLR is therefore, for bit $b_0$ of symbol $x_0$:

$$LLR(b_0) = log\left( \frac{e^{-\frac{\left|(\hat{x}_{0,I}+j\hat{x}_{0,Q})-\alpha(1+j)-\varphi_I-j\varphi_Q\right|^2}{2\sigma^2}} + e^{-\frac{\left|(\hat{x}_{0,I}+j\hat{x}_{0,Q})-\alpha(1-j)-\varphi_I-j\varphi_Q\right|^2}{2\sigma^2}}}{e^{-\frac{\left|(\hat{x}_{0,I}+j\hat{x}_{0,Q})-\alpha(-1+j)-\varphi_I-j\varphi_Q\right|^2}{2\sigma^2}} + e^{-\frac{\left|(\hat{x}_{0,I}+j\hat{x}_{0,Q})-\alpha(-1-j)-\varphi_I-j\varphi_Q\right|^2}{2\sigma^2}}} \right)$$

$$LLR(b_0) = log\left( \frac{e^{-\frac{(\hat{x}_{0,I}-\alpha-\varphi_I)^2}{2\sigma^2}} \left( e^{-\frac{(\hat{x}_{0,Q}-\alpha-\varphi_Q)^2}{2\sigma^2}} + e^{-\frac{(\hat{x}_{0,Q}+\alpha-\varphi_Q)^2}{2\sigma^2}} \right)}{e^{-\frac{(\hat{x}_{0,I}+\alpha-\varphi_I)^2}{2\sigma^2}} \left( e^{-\frac{(\hat{x}_{0,Q}-\alpha-\varphi_Q)^2}{2\sigma^2}} + e^{-\frac{(\hat{x}_{0,Q}+\alpha-\varphi_Q)^2}{2\sigma^2}} \right)} \right)$$

$$LLR(b_0) = \frac{1}{2\sigma^2}\left( (\hat{x}_{0,I} + \alpha - \varphi_I)^2 - (\hat{x}_{0,I} - \alpha - \varphi_I)^2 \right)$$

$$LLR(b_0) = \frac{2\alpha}{\sigma^2} \cdot (\hat{x}_{0,I} - \varphi_I)$$

$$\boxed{LLR(b_0) = \sqrt{2}\frac{\boldsymbol{b}\,\boldsymbol{g_e}}{\boldsymbol{b}\boldsymbol{b}^H N_0}(Re(\hat{x}_0) - \varphi_I)}$$

The LLR for the most significant bit $b_1$ is:

$$LLR(b_1) = \sqrt{2}\frac{\boldsymbol{b}\,\boldsymbol{g_e}}{\boldsymbol{b}\boldsymbol{b}^H N_0}\left(Im(\hat{x}_0) - \varphi_Q\right)$$

In the implementation, $\varphi_I$ and $\varphi_Q$ have been neglected.

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